

1.25 to 4800SPS, 24-bit Sigma-Delta ADC with PGA and Voltage Reference

FEATURES

Programmable Gain: 1/2/4/8/16/32/64/128/256
Data Rates: 1.25 to 4800SPS
RMS Noise: 35nV at 10SPS (Gain=128)
21.3 Noise Free of Bits at 10SPS (Gain=1)
Offset Drift: 5nV/°C (Gain=128)
Gain Drift: 1ppm/°C
1.17V/2.5V Internal Reference with 5ppm/°C Drift
Integral Non-Linearity: 3ppm
Internal or External Clock
Simultaneous 50Hz/60Hz Rejection
Programmable Current Sources
On-Chip Bias Voltage Generator
Burnout Current Sources
Parity Check
Power Supply
AVDD: 2.7V to 5.25V or ±2.5V
DVDD: 2.7V to 5.25V

Current: 540µA
Package: 16/20/24-lead TSSOP

APPLICATIONS

Weigh Scales
Strain Gauges
Pressure Sensors
Temperature Measurement
Industrial Process Control

DESCRIPTION

The SIG24030/1/2 are low noise, low drift, and high-resolution 24-bit analog-to-digital converters (ADC) with integrated programmable gain amplifier (PGA) and low drift on-chip voltage reference that offers high-accuracy measurement solutions for bridge sensors, thermocouples, and resistance temperature devices (RTD).

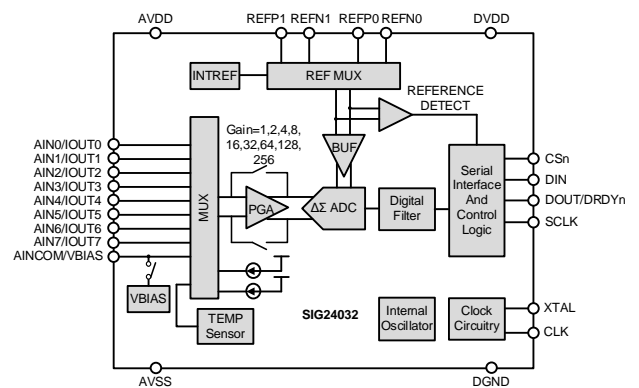
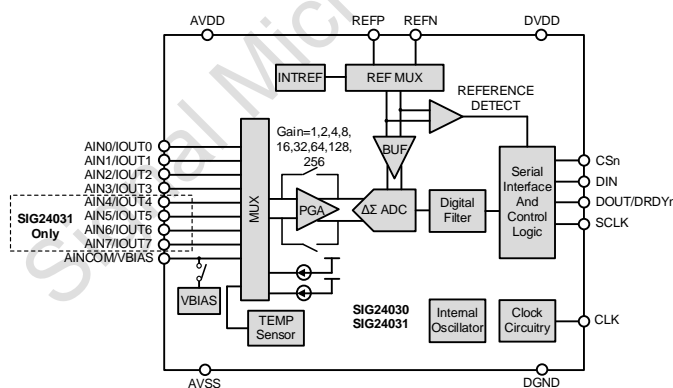
The device contains a low noise PGA with gains selected from 1, 2, 4, 8, 16, 32, 64, 128, and 256, a delta-sigma (Δ - Σ) modulator, and a programmable SINC1/SINC4 digital filter. A low drift 1.17V or 2.5V reference is integrated on chip and two matched excitation current sources (IDACs) are provided for accurate RTD measurement. The output data rate from the device can be configured to 1.25 to 4800SPS. Burnout current sources are provided at the analog inputs for sensor connection diagnosis.

Offset and gain calibration registers are provided with calibration command or direct register write to calibrate the ADC errors or overall system errors. SPI-compatible interface is used for device configuration and parity check is provided for data integrity.

The on-chip oscillator or an external clock can be used as the clock source to the device.

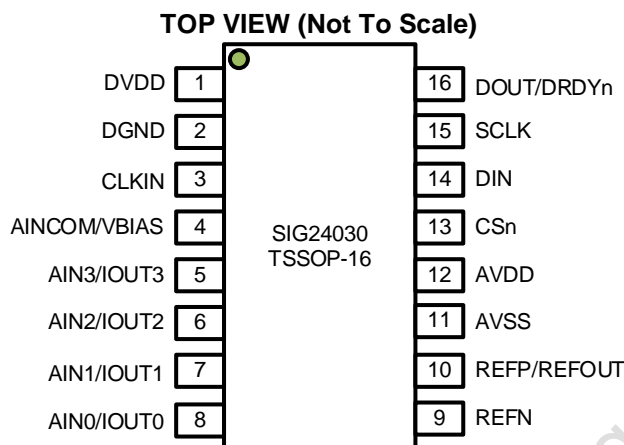
The device can operate with bipolar $\pm 1.35V$ to $\pm 2.625V$ analog power supplies, or with a single 2.7V to 5.25V analog power supply.

The SIG24030 is available in 16-lead TSSOP package, the SIG24031 is available in 20-lead TSSOP package, and the SIG24032 is available in 24-lead TSSOP package. All three devices are fully specified over the $-40^{\circ}C$ to $+125^{\circ}C$ temperature range.

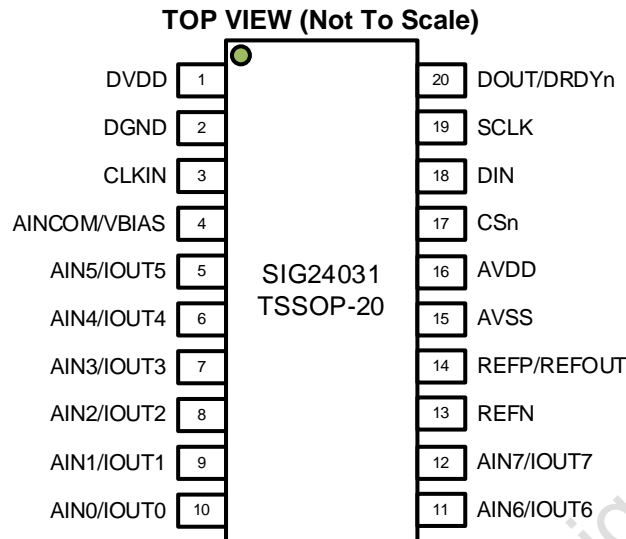


PIN CONFIGURATION and DESCRIPTIONS

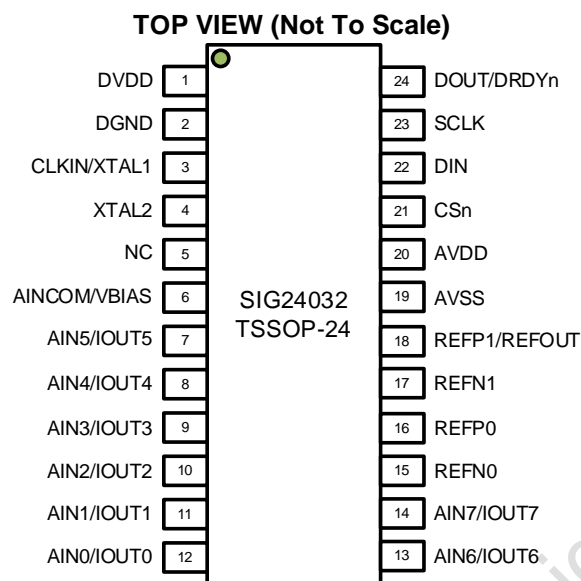
SIG24030



PIN		FUNCTION	DESCRIPTION
NO.	NAME		
1	DVDD	Digital	Digital power supply, 2.7V to 5.25V. DVDD is independent of AVDD.
2	DGND	Digital	Digital ground reference point.
3	CLKIN	Digital Input	1) Internal oscillator: Connect to DGND. 2) External clock: Connect to external clock input.
4	AINCOM/VBIAS	Analog Input	Analog input common, VBIAS.
5	AIN3/IOUT3	Analog Input	Analog input 3, IDAC3.
6	AIN2/IOUT2	Analog Input	Analog input 2, IDAC2.
7	AIN1/IOUT1	Analog Input	Analog input 1, IDAC1.
8	AIN0/IOUT0	Analog Input	Analog input 0, IDAC0.
9	REFN	Analog Input	Negative reference input.
10	REFP/REFOUT	Analog Input	Positive reference input or internal reference output.
11	AVSS	Analog	Negative analog power supply. AVSS can be taken below DVSS to provide bipolar power supplies. For example, AVSS can be tied to -2.5V and AVDD can be tied to +2.5V, providing a ±2.5V dual supplies to the ADC.
12	AVDD	Analog	Positive analog power supply. 2.7V to 5.25V relative to AVSS. AVDD is independent of DVDD.
13	CSn	Digital Input	Serial chip select. Active low.
14	DIN	Digital Input	Serial data input.
15	SCLK	Digital Input	Serial data clock.
16	DOUT/DRDYn	Digital Output	Serial data output and data ready indicator.

SIG24031


NO.	PIN		FUNCTION	DESCRIPTION
	NO.	NAME		
1		DVDD	Digital	Digital power supply, 2.7V to 5.25V. DVDD is independent of AVDD.
2		DGND	Digital	Digital ground reference point.
3		CLKIN	Digital Input	1) Internal oscillator: Connect to DGND. 2) External clock: Connect to external clock input.
4		AINCOM/VBIAS	Analog Input	Analog input common, VBIAS.
5		AIN5/IOUT5	Analog Input	Analog input 5, IDAC5.
6		AIN4/IOUT4	Analog Input	Analog input 4, IDAC4.
7		AIN3/IOUT3	Analog Input	Analog input 3, IDAC3.
8		AIN2/IOUT2	Analog Input	Analog input 2, IDAC2.
9		AIN1/IOUT1	Analog Input	Analog input 1, IDAC1.
10		AIN0/IOUT0	Analog Input	Analog input 0, IDAC0.
11		AIN6/IOUT6	Analog Input	Analog input 6, IDAC6.
12		AIN7/IOUT7	Analog Input	Analog input 7, IDAC7.
13		REFN	Analog Input	Negative reference input.
14		REFP/REFOUT	Analog Input	Positive reference input or internal reference output.
15		AVSS	Analog	Negative analog power supply. AVSS can be taken below DVSS to provide bipolar power supplies. For example, AVSS can be tied to -2.5V and AVDD can be tied to +2.5V, providing a $\pm 2.5V$ dual supplies to the ADC.
16		AVDD	Analog	Positive analog power supply. 2.7V to 5.25V relative to AVSS. AVDD is independent of DVDD.
17		CSn	Digital Input	Serial chip select. Active low.
18		DIN	Digital Input	Serial data input.
19		SCLK	Digital Input	Serial data clock.
20		DOUT/DRDYn	Digital Output	Serial data output and data ready indicator.

SIG24032


PIN		FUNCTION	DESCRIPTION
NO.	NAME		
1	DVDD	Digital	Digital power supply, 2.7V to 5.25V. DVDD is independent of AVDD.
2	DGND	Digital	Digital ground reference point.
3	CLKIN/XTAL1	Digital Input	1) Internal oscillator: Connect to DGND. 2) External clock: Connect to external clock input. 3) Crystal oscillator connection 1.
4	XTAL2	Digital Input	Crystal oscillator connection 2.
5	NC	Digital	No connection (float) or connect to DVDD/DGND.
6	AINCOM/VBIAS	Analog Input	Analog input common, VBIAS.
7	AIN5/IOUT5	Analog Input	Analog input 5, IDAC5.
8	AIN4/IOUT4	Analog Input	Analog input 4, IDAC4.
9	AIN3/IOUT3	Analog Input	Analog input 3, IDAC3.
10	AIN2/IOUT2	Analog Input	Analog input 2, IDAC2.
11	AIN1/IOUT1	Analog Input	Analog input 1, IDAC1.
12	AIN0/IOUT0	Analog Input	Analog input 0, IDAC0.
13	AIN6/IOUT6	Analog Input	Analog input 6, IDAC6.
14	AIN7/IOUT7	Analog Input	Analog input 7, IDAC7.
15	REFN0	Analog Input	Negative reference input 0.
16	REFP0	Analog Input	Positive reference input 0.
17	REFN1	Analog Input	Negative reference input 1.
18	REFP1/REFOUT	Analog Input	Positive reference input 1 or internal reference output.
19	AVSS	Analog	Negative analog power supply. AVSS can be taken below DVSS to provide bipolar power supplies. For example, AVSS can be tied to -2.5V and AVDD can be tied to +2.5V, providing a ±2.5V dual supplies to the ADC.
20	AVDD	Analog	Positive analog power supply. 2.7V to 5.25V relative to AVSS. AVDD is independent of DVDD.
21	CSn	Digital Input	Serial chip select. Active low.
22	DIN	Digital Input	Serial data input.
23	SCLK	Digital Input	Serial data clock.
24	DOUT/DRDYn	Digital Output	Serial data output and data ready indicator.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKING OPTION
SIG24030	TSSOP-16	-40°C to +125°C	SIG24030-ITSP16-RL	Reel, 5000
SIG24031	TSSOP-20	-40°C to +125°C	SIG24031-ITSP20-RL	Reel, 4500
SIG24032	TSSOP-24	-40°C to +125°C	SIG24032-ITSP24-RL	Reel, 3000

SPECIFICATIONS

Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.⁽¹⁾

		MIN	MAX	UNIT
Voltage	AVDD to AVSS	-0.3	6.5	V
	AVSS to DGND	-3	0.3	V
	DVDD to DGND	-0.3	6.5	V
	Analog input	$V_{AVSS} - 0.3$	$V_{AVDD} + 0.3$	V
	Digital input	$V_{DGND} - 0.3$	$V_{DVDD} + 0.3$	V
Current	Input current	-10	10	mA
Temperature	Junction (T_J)	-50	150	°C
	Storage (T_{stg})	-60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

SYMBOL	PARAMTER	CONDITION	VALUE	UNIT
HBM	Human-body Model	ANSI/ESDA/JEDEC JS-001	±4000	V
CDM	Charged-device model	JEDEC EIA/JS-002-2022	±2000	V



This integrated circuit can be damaged by ESD. Signal Micro recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Electrical Characteristics

Minimum/Maximum specifications apply from -40°C to +125°C. Typical specifications are at +25°C. All specifications are at $V_{AVDD}=5V$, $V_{AVSS}=0V$, $V_{DVDD}=3.3V$, $V_{REF}=2.5V$, $f_{CLK}=1.536MHz$, data rate=10SPS, and PGA Gain=1, unless otherwise noted.

PARAMETER	TEST CONDITION OR NOTES	MIN ⁽¹⁾	TYP	MAX ⁽¹⁾	UNITS
ANALOG INPUTS					
Differential Input Voltage	$V_{IN} = V_{INP} - V_{INN}$	$-V_{REF}/Gain$		$+V_{REF}/Gain$	V
Absolute Input Voltage	PGA bypass	$V_{AVSS} - 0.05$		$V_{AVDD} + 0.05$	V
	PGA enabled	$V_{AVSS} + 0.2$		$V_{AVDD} - 0.2$	V
Common MODE Input Range	PGA enabled	$V_{AVSS} + 0.2 + V_{INMAX} \cdot Gain/2$		$V_{AVDD} - 0.2 - V_{INMAX} \cdot Gain/2$	V
Absolute Input Current	PGA bypass		±5		nA
	PGA enabled		±1		nA
SYSTEM PERFORMANCE					
PGA Gain			1/2/4/8/16/32/64/128/256		V/V
Resolution			24		Bits
Data Rate		1.25		4800	SPS
Noise			See Noise Table		
Integral Nonlinearity (INL)			±3		ppm
Offset Error	All PGA gains		±256/Gain		µV
	After calibration		In order of noise		
Offset Drift vs. Temperature	All PGA gains		±256/Gain ± 3		nV/°C
Gain Error ⁽²⁾	Gain=1 to 128	-300	±100	300	ppm
	Gain=256	-450	±200	450	ppm
Gain Mismatch ⁽²⁾	Gain=1 to 128		200	350	ppm
Gain Drift vs. Temperature	All PGA gains	-3	±1	3	ppm/°C
Normal MODE Rejection (NMRR)	$f_{IN}=50/60Hz$, ±2%, data rate=10SPS		See Table 1		dB
Common MODE Rejection (CMRR)	$f_{IN}=50/60Hz$, data rate=1200SPS	100	120		dB
Power Supply Rejection (PSRR)	AVDD, AVSS	75	90		dB
	DVDD	80	120		dB
EXTERNAL REFERENCE INPUT					
Differential Reference Voltage (V_{REF})	$V_{REF} = V_{REFP} - V_{REFN}$	0.5		$V_{AVDD} - V_{AVSS} + 0.1$	V
Absolute Negative Reference Voltage (V_{REFN})		$V_{AVSS} - 0.05$		$V_{REFP} - 0.5$	V
Absolute Positive Reference Voltage (V_{REFP})		$V_{REFN} + 0.5$		$V_{AVDD} + 0.05$	V
Average Voltage Input Current			30		nA
INTERNAL VOLTAGE REFERENCE					
Reference Voltage			2.5		V
Initial Accuracy	$T_A = 25^\circ C$	-0.1%	±0.01%	+0.1%	
Voltage Temperature Drift	$T_A = -40^\circ C$ to $125^\circ C$	-20	±5	+20	ppm/°C
Power Supply Rejection			90		dB
EXCITATION CURRENT SOURCES					
Output Current	$V_{REFP} = 2.5V$		10/50/100/200/250/500/1000		µA
Compliance Voltage ⁽³⁾	IDAC ≤ 250µA	V_{AVSS}		$V_{AVDD} - 0.5$	V
	IDAC = 500µA	V_{AVSS}		$V_{AVDD} - 0.6$	V
	IDAC = 1000µA	V_{AVSS}		$V_{AVDD} - 0.8$	V
Accuracy	IDAC = 10µA	-4%	±2%	+4%	
	IDAC ≥ 50µA	-2%	±1%	+2%	
Current Mismatch	IDAC = 10µA	-3.0%	±0.60%	+3.0%	

	IDAC = 50 μ A	-1.5%	$\pm 0.25\%$	+1.5%	
	IDAC = 100 μ A	-1.2%	$\pm 0.20\%$	+1.2%	
	IDAC = 200 μ A, 250 μ A	-1.0%	$\pm 0.18\%$	+1.0%	
	IDAC = 500 μ A	-0.8%	$\pm 0.12\%$	+0.8%	
	IDAC = 1000 μ A	-0.6%	$\pm 0.1\%$	+0.6%	
Temperature Drift		-90	± 20	+90	ppm/ $^{\circ}$ C
Temperature Drift Mismatch		-30	± 5	+30	ppm/ $^{\circ}$ C
BURNOUT CURRENT SOURCES					
Current Setting			1		μ A
TEMPERATURE SENSOR					
Output Voltage			113.3		mV
Temperature Coefficient			377.6		μ V/ $^{\circ}$ C
ADC CLOCK					
External Clock	Frequency Range	1	1.536	1.6	MHz
	Duty Cycle	40%		60%	
Internal Oscillator	Nominal Frequency		1.536		MHz
	Accuracy	-2%	$\pm 0.5\%$	+2%	
DIGITAL INPUT/OUTPUT					
High-level Output Voltage (V_{OH})	$I_{OH} = 4\text{mA}$	$0.8 \cdot V_{DVDD}$			V
Low-level Output Voltage (V_{OL})	$I_{OL} = -4\text{mA}$			$0.2 \cdot V_{DVDD}$	V
High-level Input Voltage (V_{IH})		$0.7 \cdot V_{DVDD}$		V_{DVDD}	V
Low-level Input Voltage (V_{IL})		V_{DGND}		$0.3 \cdot V_{DVDD}$	V
Input Hysteresis			0.5		V
Input Leakage				± 10	μ A
POWER SUPPLY					
AVSS Voltage (V_{AVSS})		-2.625		0	V
AVDD Voltage (V_{AVDD})		$V_{AVSS} + 2.7$		$V_{AVSS} + 5.25$	V
DVDD Voltage (V_{DVDD})		2.7		5.25	V
AVDD, AVSS Current (I_{AVDD})	Buffer Off		190	250	μ A
	Buffer On		380	500	μ A
	Sleep MODE		1		μ A
DVDD Current (I_{DVDD})	Active MODE		160	240	μ A
	Sleep MODE		40		μ A
Total Power Dissipation	Buffer Off		1.5		mW
	Buffer On		2.4		mW
	Sleep MODE		0.13		mW
TEMPERATURE RANGE					
Specified temperature range		-40		125	$^{\circ}$ C
Operating temperature range		-50		125	$^{\circ}$ C
Storage temperature range		-60		150	$^{\circ}$ C

(1) Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

(2) MIN and MAX values listed for gain error are for +25 $^{\circ}$ C room temperature only.

(3) The IDAC current does not change by more than 0.01% from the nominal value when staying within the specified compliance voltage.

Timing Requirements: Serial Interface

Over the operating ambient temperature range and DVDD = 2.7V to 5.25V, unless otherwise noted.

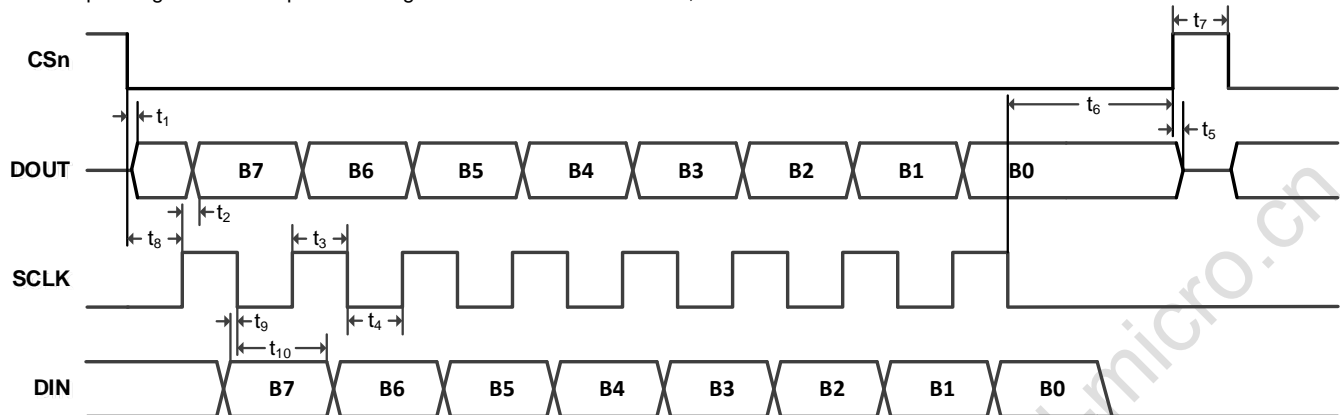


Figure 1. Serial Interface Timing Requirements

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_1	CSn falling edge to DOUT/DRDYn driven: propagation delay ⁽¹⁾		50	ns
t_2	SCLK rising edge to valid DOUT/DRDYn: propagation delay ⁽¹⁾		50	ns
t_3	SCLK high pulse width	100		ns
t_4	SCLK low pulse width	100		ns
	SCLK period	200	10^6	ns
t_5	CSn rising edge to DOUT high impedance: propagation delay		40	ns
t_6	Last SCLK falling edge to CSn rising edge: delay time	50		ns
t_7	CSn high pulse width	50		ns
t_8	CSn falling edge to first SCLK rising edge: setup time ⁽²⁾	50		ns
t_9	Valid DIN to SCLK falling edge: setup time	50		ns
t_{10}	Valid DIN to SCLK falling edge: hold time	25		ns

(1) DOUT load = 20pF || 100k Ω to DGND.

(2) CSn can be tied low.

NOISE PERFORMANCE

The noise performance of the ADC is affected by PGA gain, data rate, and digital filter setting. The following tables show the rms noise and peak-to-peak noise for SINC4 and SINC1 filters. The effective number of bits (ENOB) and noise-free bits are also listed according to Equation (1) and Equation (2):

$$\text{ENOB} = \log_2(2 \times V_{\text{REF}} / \text{Gain} / V_{\text{RMS}}) \quad (1)$$

$$\text{Noise Free Bits} = \log_2(2 \times V_{\text{REF}} / \text{Gain} / V_{\text{p-p}}) \quad (2)$$

The noise data listed in the table are typical and are generated from continuous ADC readings with differential input voltage of 0 V.

Table 3. ADC Noise in μVRMS (μVPP) at $T_A = 25^\circ\text{C}$, $V_{\text{AVDD}} = 5\text{ V}$, $V_{\text{AVSS}} = 0\text{ V}$, $V_{\text{REF}} = 2.5\text{ V}$, SINC1 Filter

Data Rate (SPS)	PGA GAIN								
	1	2	4	8	16	32	64	128	256
1.25	0.427(2.53)	0.249(1.17)	0.139(0.816)	0.078(0.391)	0.046(0.227)	0.033(0.157)	0.021(0.108)	0.019(0.089)	0.017(0.083)
2.5	0.604(3.58)	0.352(1.65)	0.197(1.15)	0.110(0.554)	0.065(0.321)	0.046(0.222)	0.030(0.153)	0.027(0.126)	0.024(0.117)
5	0.854(5.06)	0.498(2.33)	0.279(1.63)	0.156(0.783)	0.092(0.454)	0.065(0.314)	0.042(0.217)	0.038(0.179)	0.033(0.166)
6.25	0.954(5.66)	0.557(2.61)	0.311(1.83)	0.174(0.875)	0.103(0.507)	0.073(0.352)	0.047(0.242)	0.042(0.200)	0.037(0.185)
7.5	1.05(6.20)	0.610(2.86)	0.341(2.00)	0.191(0.959)	0.113(0.556)	0.080(0.385)	0.052(0.265)	0.046(0.219)	0.041(0.203)
10	1.21(7.16)	0.704(3.30)	0.394(2.31)	0.220(1.11)	0.131(0.642)	0.092(0.445)	0.060(0.306)	0.053(0.252)	0.047(0.234)
12.5	1.35(8.01)	0.788(3.69)	0.440(2.58)	0.246(1.24)	0.146(0.718)	0.103(0.497)	0.067(0.342)	0.059(0.282)	0.053(0.262)
15	1.48(8.77)	0.863(4.04)	0.482(2.83)	0.270(1.36)	0.160(0.786)	0.113(0.545)	0.073(0.375)	0.065(0.309)	0.058(0.287)
20	1.71(10.1)	0.996(4.66)	0.557(3.26)	0.312(1.57)	0.185(0.908)	0.131(0.629)	0.084(0.433)	0.075(0.357)	0.067(0.331)
25	1.91(11.3)	1.11(5.21)	0.623(3.65)	0.349(1.75)	0.207(1.01)	0.146(0.703)	0.094(0.484)	0.084(0.399)	0.074(0.370)
30	2.09(12.4)	1.22(5.71)	0.682(4.00)	0.382(1.92)	0.226(1.11)	0.160(0.770)	0.103(0.530)	0.092(0.437)	0.082(0.405)
40	2.41(14.3)	1.41(6.60)	0.788(4.62)	0.441(2.21)	0.261(1.28)	0.185(0.889)	0.119(0.612)	0.106(0.505)	0.094(0.468)
50	2.70(16.0)	1.58(7.37)	0.881(5.16)	0.493(2.48)	0.292(1.44)	0.206(0.994)	0.133(0.685)	0.119(0.565)	0.105(0.523)
60	2.96(17.5)	1.73(8.08)	0.965(5.65)	0.540(2.71)	0.320(1.57)	0.226(1.09)	0.146(0.750)	0.130(0.618)	0.115(0.573)
80	3.41(20.3)	1.99(9.33)	1.11(6.53)	0.623(3.13)	0.370(1.82)	0.261(1.26)	0.168(0.866)	0.150(0.714)	0.133(0.662)
100	3.82(22.6)	2.23(10.4)	1.25(7.30)	0.697(3.50)	0.413(2.03)	0.292(1.41)	0.188(0.968)	0.168(0.798)	0.149(0.740)
120	4.28(22.6)	2.48(12.2)	1.39(6.93)	0.834(4.02)	0.482(2.57)	0.322(1.64)	0.222(1.20)	0.196(0.952)	0.171(0.957)
125	4.70(22.9)	3.34(18.0)	1.62(7.00)	0.891(4.80)	0.511(2.51)	0.324(1.97)	0.257(1.26)	0.194(1.08)	0.185(0.962)
150	4.41(28.9)	2.73(12.1)	1.63(8.72)	0.859(5.59)	0.513(2.98)	0.335(1.77)	0.236(1.32)	0.210(1.15)	0.196(0.970)
200	5.38(25.9)	3.15(16.8)	1.68(10.2)	0.974(5.29)	0.626(3.85)	0.373(1.79)	0.268(1.51)	0.223(1.11)	0.211(1.04)
240	5.55(34.3)	3.31(17.6)	1.77(11.5)	1.05(5.40)	0.584(3.52)	0.437(2.86)	0.331(2.04)	0.252(1.55)	0.226(1.27)
250	5.81(34.6)	4.07(27.3)	2.15(13.3)	1.19(7.00)	0.725(4.32)	0.494(2.86)	0.348(2.30)	0.277(1.54)	0.249(1.55)
300	6.14(36.4)	3.57(17.1)	2.06(12.3)	1.11(6.03)	0.700(3.67)	0.443(2.50)	0.335(1.84)	0.272(1.58)	0.253(1.39)
400	7.16(42.0)	4.30(25.5)	2.20(13.9)	1.25(7.60)	0.733(8.94)	0.493(3.16)	0.392(2.17)	0.315(2.20)	0.276(1.83)
500	8.67(56.3)	5.43(33.7)	2.56(16.5)	1.50(9.76)	0.878(5.36)	0.624(4.47)	0.447(2.75)	0.341(1.85)	0.313(1.90)
600	8.42(51.2)	4.98(29.1)	2.56(15.0)	1.42(8.31)	0.894(6.05)	0.614(3.58)	0.439(2.65)	0.372(2.14)	0.333(2.02)
1000	9.66(58.4)	6.08(39.3)	3.17(18.8)	1.83(11.0)	1.09(7.17)	0.703(5.48)	0.496(3.03)	0.406(2.47)	0.369(2.44)
1200	9.64(64.4)	5.93(41.1)	3.01(18.7)	1.75(11.0)	1.06(7.32)	0.704(4.46)	0.493(3.02)	0.426(2.75)	0.387(2.47)
2000	31.1(218)	16.0(109)	8.33(60.3)	4.20(30.5)	2.34(17.2)	1.33(9.64)	0.818(5.20)	0.617(4.26)	0.547(3.31)
2400	30.8(219)	16.6(118)	8.54(64.4)	4.19(28.1)	2.31(15.3)	1.31(8.88)	0.841(5.99)	0.645(4.16)	0.552(3.85)
4000	322(2500)	160(1340)	81.7(644)	39.9(286)	19.6(156)	9.53(66.3)	5.09(36.1)	2.58(17.2)	1.42(9.42)
4800	320(2810)	159(1320)	77.9(673)	38.9(286)	19.9(147)	9.62(72.2)	4.97(37.6)	2.58(19.2)	1.44(10.1)

Table 4. ADC ENOB (Noise Free Bits) at $T_A = 25^\circ\text{C}$, $V_{\text{AVDD}} = 5\text{ V}$, $V_{\text{AVSS}} = 0\text{ V}$, $V_{\text{REF}} = 5\text{ V}$, SINC1 Filter

Data Rate (SPS)	PGA GAIN								
	1	2	4	8	16	32	64	128	256
1.25	24.5(22.2)	24.3(22.0)	24.0(21.5)	24.0(21.6)	23.5(21.0)	23.1(20.8)	22.6(20.4)	21.9(19.3)	21.1(19.0)
2.5	24.0(21.7)	23.8(21.5)	23.5(21.0)	23.5(21.1)	23.0(20.5)	22.6(20.3)	22.1(19.9)	21.4(18.8)	20.6(18.5)
5	23.5(21.2)	23.3(21.0)	23.0(20.5)	23.0(20.6)	22.5(20.0)	22.1(19.8)	21.6(19.4)	20.9(18.3)	20.1(18.0)
6.25	23.4(21.0)	23.2(20.8)	22.9(20.4)	22.8(20.4)	22.4(19.9)	21.9(19.6)	21.4(19.2)	20.8(18.2)	19.9(17.8)
7.5	23.2(20.9)	23.0(20.7)	22.7(20.3)	22.7(20.3)	22.2(19.7)	21.8(19.5)	21.3(19.1)	20.6(18.0)	19.8(17.7)
10	23.0(20.7)	22.8(20.5)	22.5(20.0)	22.5(20.1)	22.0(19.5)	21.6(19.3)	21.1(18.9)	20.4(17.8)	19.6(17.5)
12.5	22.9(20.5)	22.7(20.3)	22.4(19.9)	22.3(19.9)	21.9(19.4)	21.4(19.1)	20.9(18.7)	20.3(17.7)	19.4(17.3)
15	22.7(20.4)	22.5(20.2)	22.2(19.8)	22.2(19.8)	21.7(19.2)	21.3(19.0)	20.8(18.6)	20.1(17.5)	19.3(17.2)
20	22.5(20.2)	22.3(20.0)	22.0(19.5)	22.0(19.6)	21.5(19.0)	21.1(18.8)	20.6(18.4)	19.9(17.3)	19.1(17.0)
25	22.4(20.0)	22.2(19.8)	21.9(19.4)	21.8(19.4)	21.4(18.9)	20.9(18.6)	20.4(18.2)	19.8(17.2)	18.9(16.8)
30	22.2(19.9)	22.0(19.7)	21.7(19.3)	21.7(19.3)	21.2(18.7)	20.8(18.5)	20.3(18.1)	19.6(17.0)	18.8(16.7)
40	22.0(19.7)	21.8(19.5)	21.5(19.0)	21.5(19.1)	21.0(18.5)	20.6(18.3)	20.1(17.9)	19.4(16.8)	18.6(16.5)
50	21.9(19.5)	21.7(19.3)	21.4(18.9)	21.3(18.9)	20.9(18.4)	20.4(18.1)	19.9(17.7)	19.3(16.7)	18.4(16.3)
60	21.7(19.4)	21.5(19.2)	21.2(18.8)	21.2(18.8)	20.7(18.2)	20.3(18.0)	19.8(17.6)	19.1(16.5)	18.3(16.2)
80	21.5(19.2)	21.3(19.0)	21.0(18.5)	21.0(18.6)	20.5(18.0)	20.1(17.8)	19.6(17.4)	18.9(16.3)	18.1(16.0)
100	21.4(19.0)	21.2(18.8)	20.9(18.4)	20.8(18.4)	20.4(17.9)	19.9(17.6)	19.4(17.2)	18.8(16.2)	17.9(15.8)
120	21.1(18.7)	20.8(18.2)	20.8(18.4)	20.5(18.0)	20.3(17.7)	15.5(12.3)	19.4(17.2)	18.6(16.3)	17.7(15.3)
125	20.9(18.7)	20.4(18.2)	20.6(18.1)	20.5(18.0)	20.2(17.8)	19.8(17.5)	19.3(16.9)	18.7(16.4)	17.8(15.5)
150	21.0(18.5)	20.8(18.2)	20.7(18.1)	20.7(18.2)	20.2(17.6)	19.8(17.5)	19.2(16.7)	18.5(16.1)	17.7(15.4)
200	20.9(18.3)	20.6(18.0)	20.6(18.0)	20.6(19.3)	20.0(17.6)	19.6(17.2)	19.0(16.5)	18.4(16.0)	17.6(15.0)
240	20.7(18.2)	20.5(18.0)	20.3(17.7)	20.2(17.5)	19.8(17.0)	19.5(17.0)	19.0(16.3)	18.2(15.7)	17.3(14.7)
250	20.5(18.0)	20.2(17.9)	20.2(17.8)	20.1(17.5)	19.7(17.1)	19.2(16.8)	18.7(16.3)	18.1(15.6)	17.3(15.0)
300	20.6(18.2)	20.3(17.8)	20.2(17.7)	20.1(17.6)	19.7(17.3)	19.4(16.9)	18.8(16.2)	18.1(15.5)	17.3(14.8)
400	20.5(17.8)	20.2(17.4)	20.0(17.2)	19.9(17.3)	19.5(16.9)	19.2(16.6)	18.7(16.3)	18.0(15.4)	17.0(14.3)
500	20.2(17.6)	19.8(17.2)	19.8(17.2)	19.7(17.1)	19.4(16.6)	19.0(16.2)	18.4(15.7)	17.8(15.2)	17.0(14.4)
600	20.2(17.6)	19.9(17.3)	19.9(17.2)	19.6(17.0)	19.4(16.7)	19.0(16.3)	18.5(15.9)	17.7(15.2)	16.9(14.3)
1000	19.8(17.0)	19.5(16.8)	19.5(16.9)	19.4(16.8)	19.1(16.3)	18.8(15.9)	18.3(15.4)	17.5(14.8)	16.7(13.9)
1200	19.8(17.1)	19.7(16.9)	19.5(16.8)	19.4(16.6)	19.1(16.5)	18.7(15.9)	18.2(15.5)	17.5(15.0)	16.7(14.0)
2000	17.4(14.4)	17.4(14.6)	17.4(14.6)	17.4(14.5)	17.3(14.6)	17.2(14.5)	17.0(14.2)	16.7(14.0)	16.1(13.3)
2400	17.4(14.2)	17.3(14.6)	17.3(14.5)	17.3(14.4)	17.4(14.5)	17.2(14.3)	17.1(14.1)	16.7(13.9)	16.0(13.2)
4000	13.9(11.2)	14.0(11.1)	14.0(10.9)	14.0(11.0)	14.0(11.0)	14.0(11.0)	14.0(11.0)	14.0(11.2)	13.9(11.1)
4800	13.9(10.9)	13.9(10.9)	13.9(11.1)	13.9(11.0)	13.9(10.8)	14.0(11.0)	13.9(11.0)	13.9(11.1)	13.9(11.0)

REVISION HISTORY

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
July 12, 2022		Initial release.

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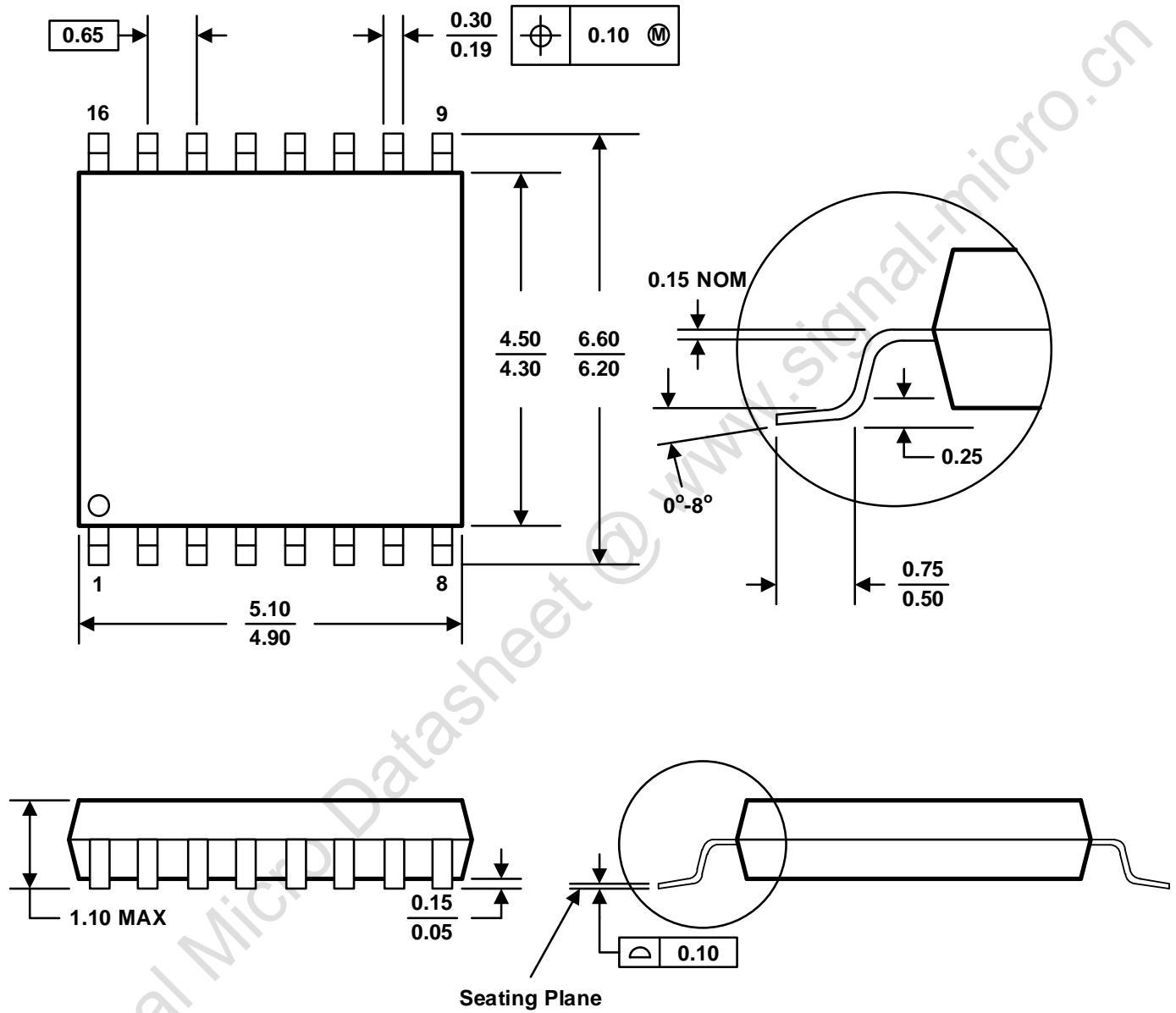
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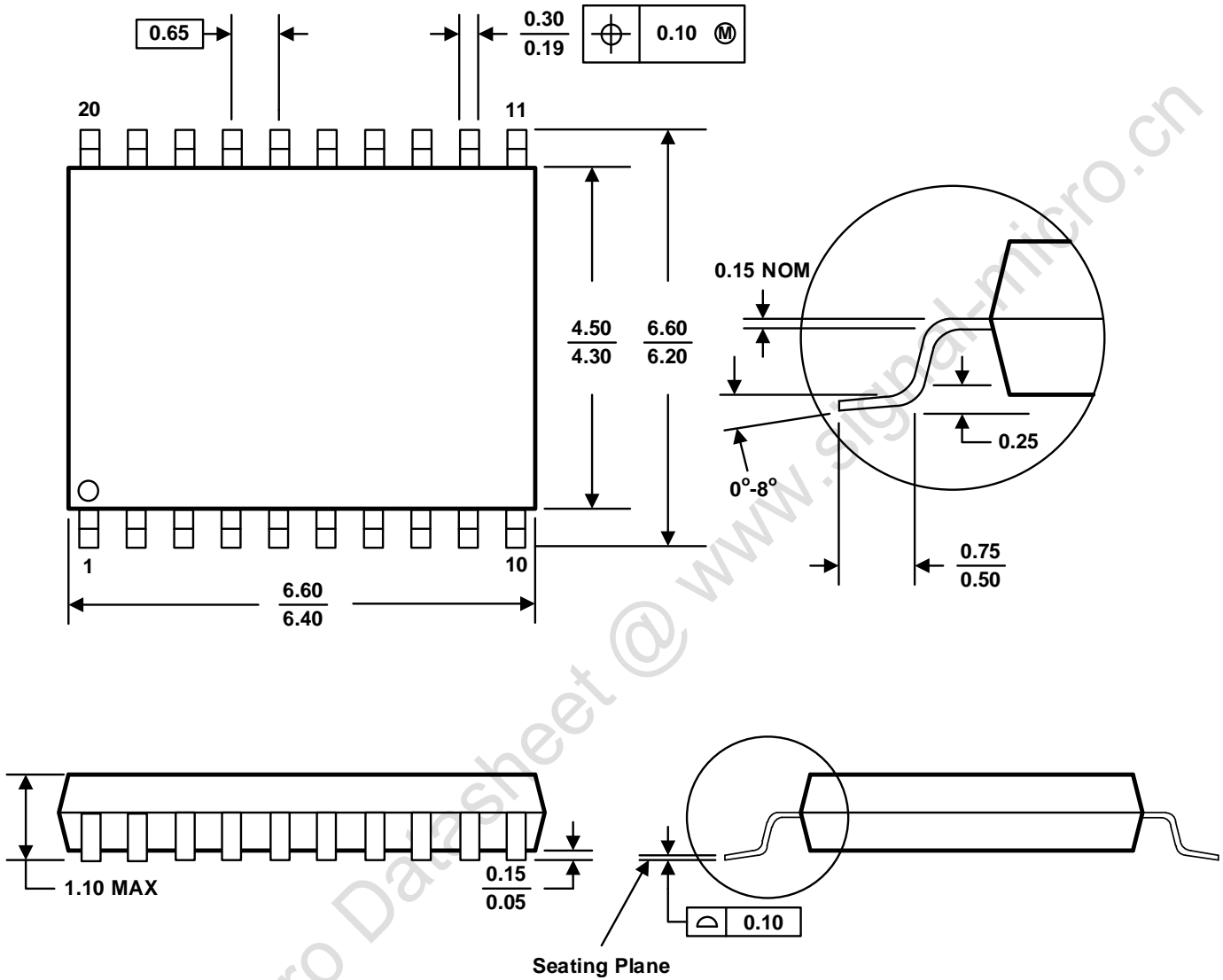
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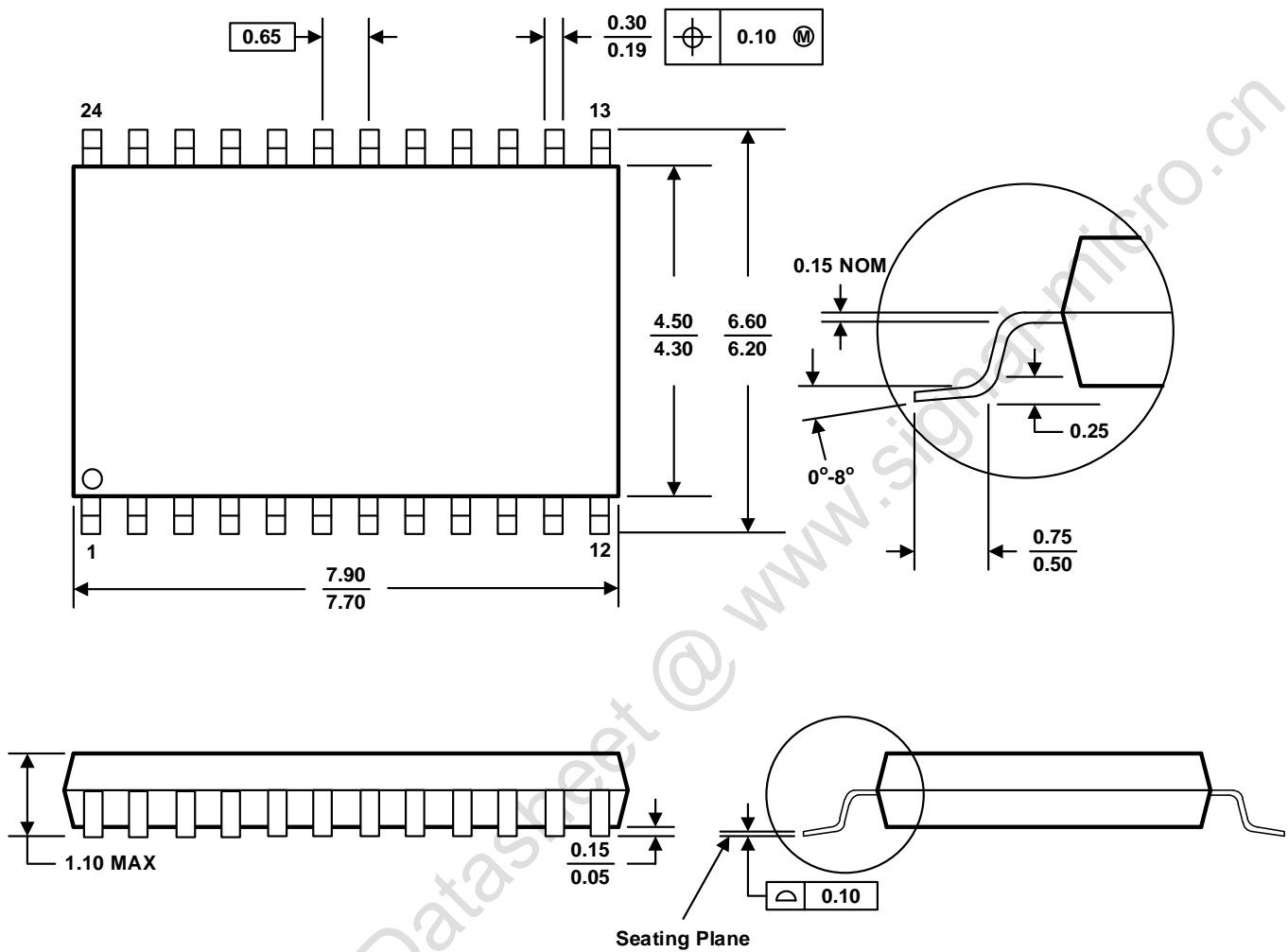
TSSOP-16



- A. Compliant to JEDEC STANDARDS MO-153-AD.
- B. All linear dimensions are in millimeters.
- C. This drawing is subject to change without notice.

TSSOP-20


- A. Compliant to JEDEC STANDARDS MO-153-AD.
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