SIG2430: 10 to 2400SPS, 24-bit Sigma-Delta ADC with PGA

FEATURES

Programmable Gain: 1/2/4/8/16/32/64/128
Data Rates: 10/20/50/200/400/1200/2400SPS
RMS Noise: 22nV at 10SPS (Gain=128)
23.9 Effective Number of Bits at 10SPS (Gain=1)
Offset Drift: 5nV/°C (Gain=128)
Gain Drift: 1ppm/°C
Integral Non-Linearity: 3ppm
Internal or External Clock
Burnout Current Sources
Parity Check
Power Supply
- **AVDD: 2.7V to 5.25V or ±2.5V**
- **DVDD: 2.7V to 5.25V**

Current: 1.5mA
Package: 16-lead TSSOP

APPLICATIONS

Weigh Scales
Strain Gauges
Pressure Sensors
Temperature Measurement
Industrial Process Control

DESCRIPTION

The SIG2430 is a low noise, low drift, and high-resolution 24-bit analog-to-digital converter (ADC) with integrated programmable gain amplifier (PGA) that offers high-accuracy measurement solutions for bridge sensors, thermocouples, and resistance temperature devices (RTD).

The device contains a low noise PGA with gains selected from 1, 2, 4, 8 16, 32, 64, and 128, a delta-sigma (Δ-Σ) modulator, and a programmable SINC1/SINC4 digital filter. The output data rate from the device can be configured to 10, 20, 50, 200, 400, 1200, and 2400SPS. Burnout current sources are provided at the analog inputs for sensor connection diagnosis.

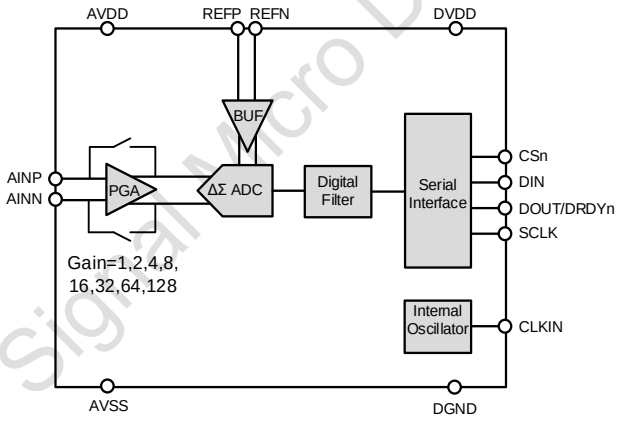
Offset and gain calibration registers are provided with calibration command or direct register write to calibrate the ADC errors or overall system errors. SPI-compatible interface is used for device configuration and parity check is provided for data integrity.

The on-chip oscillator, an external clock, or an external crystal can be used as the clock source to the device.

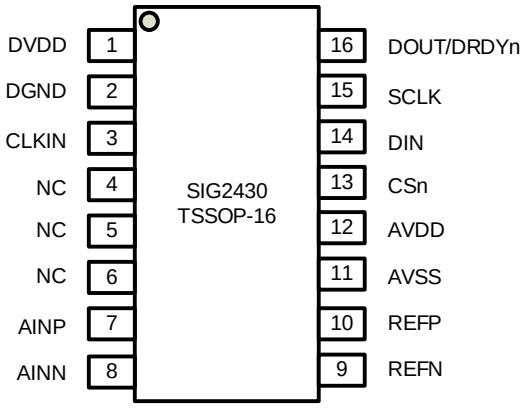
The device can operate with bipolar ±1.35V to ±2.625V analog power supplies, or with a single 2.7V to 5.25V analog power supply.

The SIG2430 is available in 16-lead TSSOP package and is fully specified over the -40°C to +125°C temperature range.

Function Block Diagram

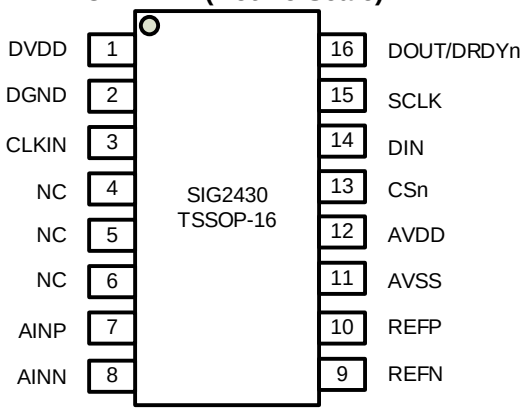


TSSOP-16



PIN CONFIGURATION and DESCRIPTIONS

TOP VIEW (Not To Scale)



PIN		FUNCTION	DESCRIPTION
NO.	NAME		
1	DVDD	Digital	Digital power supply, 2.7V to 5.25V. DVDD is independent of AVDD.
2	DGND	Digital	Digital ground reference point.
3	CLKIN	Digital Input	1) Internal oscillator: Connect to DGND. 2) External clock: Connect to external clock input.
4	NC	Digital	No connection (float) or connect to DVDD/DGND.
5	NC	Digital	No connection (float) or connect to DVDD/DGND.
6	NC	Digital	No connection (float) or connect to DVDD/DGND.
7	AINP	Analog Input	Positive analog input.
8	AINN	Analog Input	Negative analog input.
9	REFN	Analog Input	Negative reference input.
10	REFP	Analog Input	Positive reference input.
11	AVSS	Analog	Negative analog power supply. AVSS can be taken below DVSS to provide bipolar power supplies. For example, AVSS can be tied to –2.5V and AVDD can be tied to +2.5V, providing a ±2.5V dual supplies to the ADC.
12	AVDD	Analog	Positive analog power supply. 2.7V to 5.25V relative to AVSS. AVDD is independent of DVDD.
13	CSn	Digital Input	Serial chip select. Active low.
14	DIN	Digital Input	Serial data input.
15	SCLK	Digital Input	Serial data clock.
16	DOUT/DRDYn	Digital Output	Serial data output and data ready indicator.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKING OPTION
SIG2430	TSSOP-16	-40°C to +125°C	SIG2430-ITSP16-RL	Reel, 5000

SPECIFICATIONS

Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
Voltage	AVDD to AVSS	–0.3	6.5	V
	AVSS to DGND	–3	0.3	V
	DVDD to DGND	–0.3	6.5	V
	Analog input	V_{AVSS} – 0.3	V_{AVDD} + 0.3	V
	Digital input	V_{DGND} – 0.3	V_{DVDD} + 0.3	V
Current	Input current	–10	10	mA
Temperature	Junction (T_J)	–50	150	°C
	Storage (T_{stg})	-60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

SYMBOL	PARAMTER	CONDITION	VALUE	UNIT
HBM	Human-body model	ANSI/ESDA/JEDEC JS-001	±8000	V
MM	Machine model	JEDEC EIA/JESD22-A115C	±400	V

This integrated circuit can be damaged by ESD. Signal Micro recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Electrical Characteristics

Minimum/Maximum specifications apply from -40˚C to +125˚C. Typical specifications are at +25˚C. All specification are at V_{AVDD}=5V, V_{AVSS}=0V, V_{DVDD}=3.3V, V_{REF}=2.5V, f_{CLK}=2.4576MHz, data rate=10SPS, and PGA Gain=1, unless otherwise noted.

PARAMETER	TEST CONDITION OR NOTES	MIN(1)	TYP	MAX(1)	UNITS
ANALOG INPUTS					
Differential Input Voltage	$V_{IN} = V_{INP} – V_{INN}$	$–V_{REF}$/Gain		$+V_{REF}$/Gain	V
Absolute Input Voltage	PGA bypass	$V_{AVSS} – 0.05$		$V_{AVDD} + 0.05$	V
	PGA enabled	$V_{AVSS} + 0.5$		$V_{AVDD} – 0.5$	
Common Mode Input Range	PGA enabled	$V_{AVSS} + 0.5 + \lvert V_{INMAX}\rvert \cdot Gain/2$		$V_{AVDD} – 0.5 – \lvert V_{INMAX}\rvert \cdot Gain/2$	V
Absolute Input Current	PGA bypass		±50		nA
	PGA enabled		±1		nA
SYSTEM PERFORMANCE					
PGA Gain			1/2/4/8/16/32/64/128		V/V
Resolution			24		Bits
Data Rate		10		2400	SPS
Noise			See Noise Table		
Integral Nonlinearity (INL)			±3		ppm
Offset Error	All PGA gains		±256/Gain		µV
Offset Drift vs. Temperature	All PGA gains		±256/Gain ± 3		nV/°C
Gain Error	All PGA gains		±0.01		%
Gain Drift vs. Temperature	All PGA gains	-5	±1	5	ppm/°C
Normal Mode Rejection (NMRR)	f_{IN}=50/60Hz, ±2%, data rate=10SPS		See Table 12		dB
Common Mode Rejection (CMRR)	f_{IN}=50/60Hz, data rate=1200SPS	100	120		dB
Power Supply Rejection(2) (PSRR)	AVDD, AVSS	75	90		dB
	DVDD	80	120		dB
REFERENCE INPUT					
Differential Reference Voltage (V_{REF})	$V_{REF} = V_{REFP} – V_{REFN}$	0.5		$V_{AVDD} – V_{AVSS} + 0.1$	V
Absolute Negative Reference Voltage (V_{REFN})		$V_{AVSS} – 0.05$		$V_{REFP} – 0.5$	V
Absolute Positive Reference Voltage (V_{REFP})		$V_{REFN} + 0.5$		$V_{AVDD} + 0.05$	V
Average Voltage Input Current			50		nA
Burnout Current Sources					
Current Setting			2		µA
ADC CLOCK					
External Clock	Frequency Range	1	2.4576	2.5	MHz
	Duty Cycle	40%		60%	
Internal Oscillator	Nominal Frequency		2.4576		MHz
	Accuracy	–3%	±0.5%	3%	
DIGITAL INPUT/OUTPUT					
High-level Output Voltage (V_{OH})	I_{OH} = 1mA	$0.8 \cdot V_{DVDD}$			V
Low-level Output Voltage (V_{OL})	I_{OL} = –1mA			$0.2 \cdot V_{DVDD}$	V
High-level Input Voltage (V_{IH})		$0.7 \cdot V_{DVDD}$		V_{DVDD}	V
Low-level Input Voltage (V_{IL})		V_{DGND}		$0.3 \cdot V_{DVDD}$	V
Input Hysteresis			0.5		V
Input Leakage				±10	µA
POWER SUPPLY					
AVSS Voltage (V_{AVSS})		–2.625		0	V
AVDD Voltage (V_{AVDD})		$V_{AVSS} + 2.7$		$V_{AVSS} + 5.25$	V
DVDD Voltage (V_{DVDD})		2.7		5.25	V

AVDD, AVSS Current (I_{AVDD})	PGA Bypass		0.6	0.9	mA
	PGA Enabled		1.3	1.8	mA
	Sleep Mode		0		µA
DVDD Current (I_{DVDD})	Active Mode		220	300	µA
	Sleep Mode		50		µA
Total Power Dissipation	PGA Bypass		3.6		mW
	PGA Enabled		7		mW
	Sleep Mode		0.16		mW
TEMPERATURE RANGE					
Specified temperature range		–40		125	°C
Operating temperature range		–50		125	°C
Storage temperature range		–60		150	°C

(1) Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
(2) Power supply rejection is specified DC change in voltage.

Timing Requirements: Serial Interface

Over the operating ambient temperature range and DVDD = 2.7V to 5.25V, unless otherwise noted.

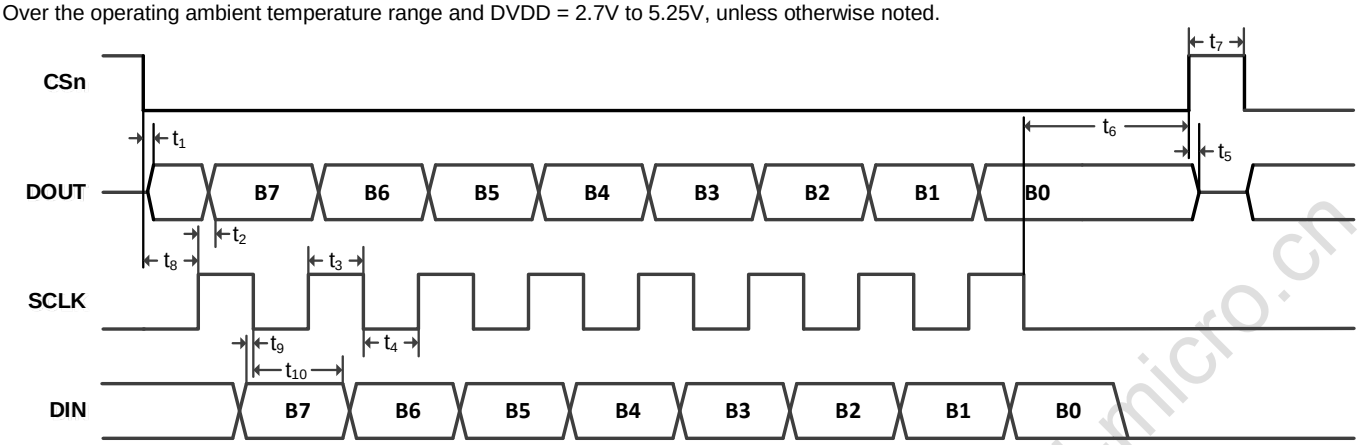


Figure 1. Serial Interface Timing Requirements

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_1	CSn falling edge to DOUT/DRDYn driven: propagation delay(1)		50	ns
t_2	SCLK rising edge to valid DOUT/DRDYn: propagation delay(1)		50	ns
t_3	SCLK high pulse width	100		ns
t_4	SCLK low pulse width	100		ns
	SCLK period	200	10^6	ns
t_5	CSn rising edge to DOUT high impedance: propagation delay		40	ns
t_6	Last SCLK falling edge to CSn rising edge: delay time	50		ns
t_7	CSn high pulse width	50		ns
t_8	CSn falling edge to first SCLK rising edge: setup time(2)	50		ns
t_9	Valid DIN to SCLK falling edge: setup time	50		ns
t_{10}	Valid DIN to SCLK falling edge: hold time	25		ns

(1) DOUT load = 20pF || 100kΩ to DGND.
(2) CSn can be tied low.

NOISE PERFORMANCE

The noise performance of the ADC is affected by PGA gain, data rate, and digital filter setting. The following tables show the rms noise and peak-to-peak noise for SINC4 and SINC1 filters. The effective number of bits (ENOB) and noise-free bits are also listed according to Equation (1) and Equation (2):

$$\text{ENOB} = \log_2(2 \times V_{REF}/\text{Gain}/V_{RMS}) \quad (1)$$

$$\text{Noise Free Bits} = \log_2(2 \times V_{REF}/\text{Gain}/V_{p\text{-}p}) \quad (2)$$

The noise data listed in the table are typical and are generated from continuous ADC readings with differential input voltage of 0 V.

Table 1. ADC Noise in μVRMS (μVPP) at T_A = 25°C, V_{AVDD} = 5 V, V_{AVSS} = 0 V, V_{REF} = 2.5 V, SINC4 Filter

Data Rate (SPS)	PGA GAIN							
	1	2	4	8	16	32	64	128
10	0.589(3.49)	0.372(2.07)	0.196(1.13)	0.098(0.648)	0.056(0.401)	0.039(0.208)	0.029(0.169)	0.022(0.126)
20	0.833(4.93)	0.527(2.93)	0.277(1.60)	0.138(0.916)	0.080(0.566)	0.055(0.294)	0.040(0.239)	0.031(0.178)
50	1.32(7.80)	0.833(4.64)	0.438(2.53)	0.219(1.45)	0.126(0.896)	0.088(0.464)	0.064(0.379)	0.049(0.281)
200	2.64(15.6)	1.67(9.27)	0.877(5.06)	0.438(2.90)	0.252(1.79)	0.175(0.928)	0.128(0.757)	0.099(0.561)
400	3.73(22.1)	2.36(13.1)	1.24(7.15)	0.619(4.10)	0.357(2.53)	0.248(1.31)	0.181(1.07)	0.140(0.794)
1200	6.56(40.2)	3.96(27.3)	2.02(13.6)	1.13(7.86)	0.650(4.41)	0.422(3.38)	0.309(2.34)	0.234(1.37)
2400	10.2(69.1)	6.16(43.2)	3.19(19.0)	1.67(12.2)	0.973(7.45)	0.614(4.55)	0.444(2.95)	0.360(2.95)

Table 2. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 5 V, V_{AVSS} = 0 V, V_{REF} = 5 V, SINC4 Filter

Data Rate (SPS)	PGA GAIN							
	1	2	4	8	16	32	64	128
10	23.9(21.3)	23.8(21.3)	23.7(21.1)	23.6(21.4)	23.3(20.7)	22.9(20.4)	22.4(19.9)	21.7(18.8)
20	23.4(20.8)	23.3(20.8)	23.2(20.6)	23.1(20.9)	22.8(20.2)	22.4(19.9)	21.9(19.4)	21.2(18.3)
50	22.7(20.2)	22.6(20.1)	22.5(20.0)	22.4(20.2)	22.1(19.5)	21.7(19.2)	21.2(18.7)	20.6(17.7)
200	21.7(19.2)	21.6(19.1)	21.5(19.0)	21.4(19.2)	21.1(18.5)	20.7(18.2)	20.2(17.7)	19.6(16.7)
400	21.2(18.7)	21.1(18.6)	21.0(18.5)	20.9(18.7)	20.6(18.0)	20.2(17.7)	19.7(17.2)	19.1(16.2)
1200	20.6(17.9)	20.3(17.6)	20.2(17.5)	20.1(17.5)	19.9(17.4)	19.5(16.8)	19.0(16.3)	18.2(15.6)
2400	19.5(16.8)	19.4(16.7)	19.3(16.6)	19.3(16.3)	19.1(16.3)	18.9(16.1)	18.3(15.5)	17.8(15.0)

Table 3. ADC Noise in μVRMS (μVPP) at T_A = 25°C, V_{AVDD} = 5 V, V_{AVSS} = 0 V, V_{REF} = 2.5 V, SINC1 Filter

Data Rate (SPS)	PGA GAIN							
	1	2	4	8	16	32	64	128
10	0.819(4.99)	0.478(2.92)	0.251(1.44)	0.140(0.736)	0.080(0.627)	0.053(0.320)	0.038(0.254)	0.031(0.185)
20	1.16(7.06)	0.676(4.13)	0.355(2.03)	0.199(1.04)	0.114(0.887)	0.075(0.452)	0.054(0.359)	0.044(0.262)
50	1.83(11.2)	1.07(6.53)	0.562(3.21)	0.314(1.65)	0.180(1.40)	0.119(0.715)	0.085(0.568)	0.069(0.415)
200	3.66(22.3)	2.14(13.1)	1.12(6.43)	0.628(3.29)	0.360(2.81)	0.238(1.43)	0.170(1.14)	0.139(0.829)
400	5.18(31.6)	3.03(18.5)	1.59(9.09)	0.888(4.66)	0.509(3.97)	0.337(2.02)	0.240(1.61)	0.196(1.17)
1200	8.02(51.9)	4.86(34.7)	2.49(18.8)	1.41(8.79)	0.776(5.27)	0.518(3.06)	0.367(2.26)	0.305(2.01)
2400	10.2(69.1)	6.16(43.2)	3.19(19.0)	1.67(12.2)	0.973(7.45)	0.614(4.55)	0.444(2.95)	0.360(2.95)

Table 4. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 5 V, V_{AVSS} = 0 V, V_{REF} = 5 V, SINC1 Filter

Data Rate (SPS)	PGA GAIN							
	1	2	4	8	16	32	64	128
10	23.4(20.6)	23.3(20.6)	23.2(20.9)	23.1(20.5)	22.9(20.4)	22.5(19.9)	21.9(19.5)	21.3(18.9)
20	22.9(20.1)	22.8(20.1)	22.7(20.4)	22.6(20.0)	22.4(19.9)	22.0(19.4)	21.4(19.0)	20.8(18.4)
50	22.2(19.5)	22.1(19.5)	22.1(19.7)	21.9(19.4)	21.7(19.3)	21.3(18.7)	20.7(18.3)	20.1(17.8)
200	21.2(18.5)	21.1(18.5)	21.1(18.7)	20.9(18.4)	20.7(18.3)	20.3(17.7)	19.7(17.3)	19.1(16.8)
400	20.7(18.0)	20.6(18.0)	20.6(18.2)	20.4(17.9)	20.2(17.8)	19.8(17.2)	19.2(16.8)	18.6(16.3)
1200	20.1(17.2)	19.9(17.1)	19.9(17.2)	19.8(17.1)	19.5(16.8)	19.2(16.6)	18.7(15.9)	18.0(15.3)
2400	19.5(16.8)	19.4(16.7)	19.3(16.6)	19.3(16.3)	19.1(16.3)	18.9(16.1)	18.3(15.5)	17.8(15.0)

REVISION HISTORY

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

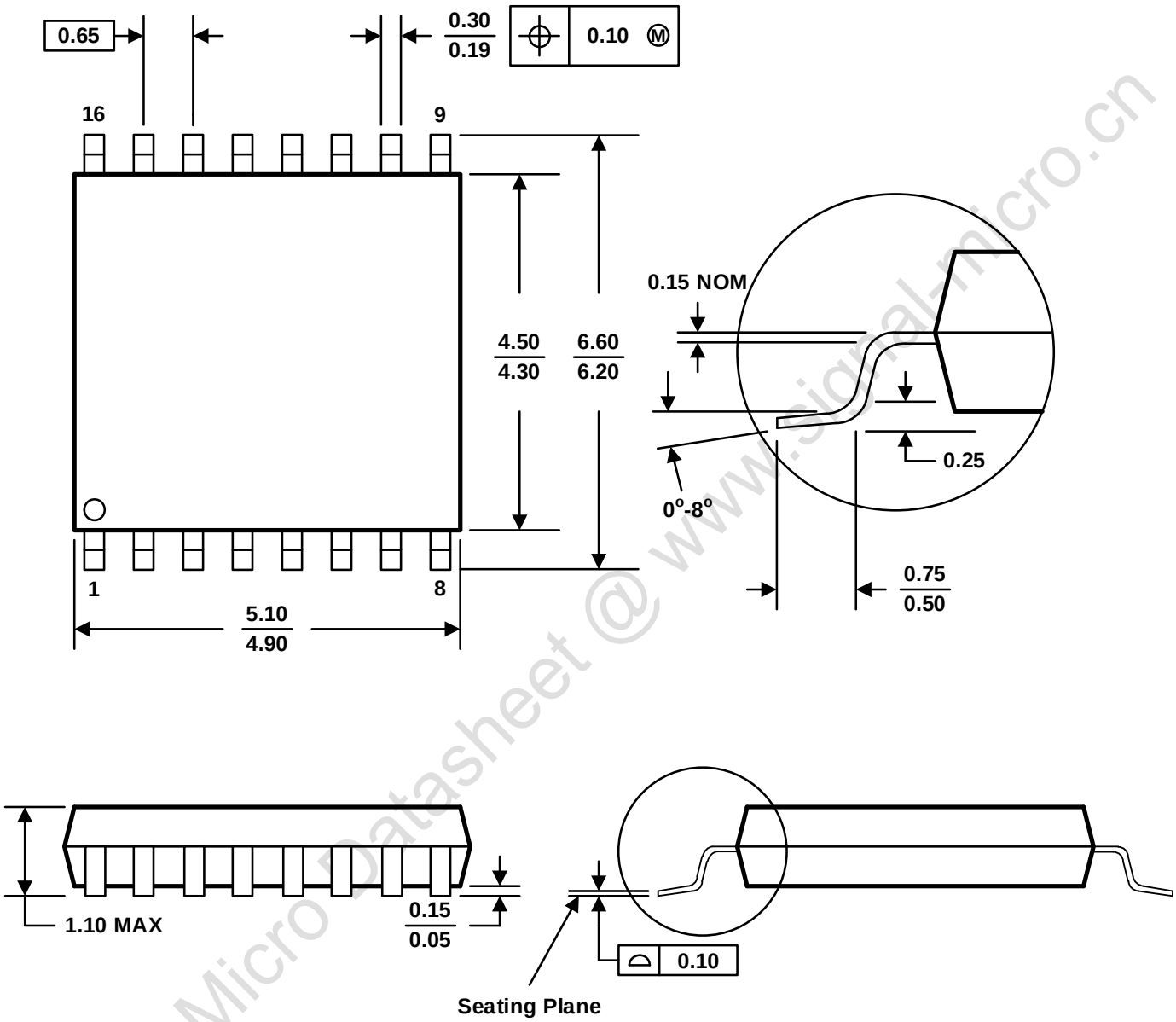
DATE	REVISION	CHANGE
Jan. 20, 2020		Initial release.
Oct. 28, 2020		Update Table 9. ADC commands.
May 25, 2021		Correct the description of bit 23 in MODE Register.

DISCLAIMER

Signal Micro reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

All trademarks and registered trademarks are the property of their respective owners.

PACKAGE OUTLINE DIMENSIONS



A. Compliant to JEDEC STARDARDS MO-153-AD.
B. All linear dimensions are in millimeters.
C. This drawing is subject to change without notice.