8-Channel, 24-bit Sigma-Delta ADC with PGA and Reference

FEATURES

4 Power Modes
RMS Noise @ Gain=128:
- **Low power: 13nV at 1.17SPS**
- **Mid1 power: 14nV at 2.34SPS**
- **Mid2 power: 17nV at 4.69SPS**
- **Full power: 18nV at 9.38SPS**

Up to 22.5 noise-free bits at all power modes (Gain=1)
Output Data Rates:
- **Low power: 1.17SPS to 2400SPS**
- **Mid1 power: 2.34SPS to 4800SPS**
- **Mid2 power: 4.69SPS to 9600SPS**
- **Full power: 9.38SPS to 19200SPS**

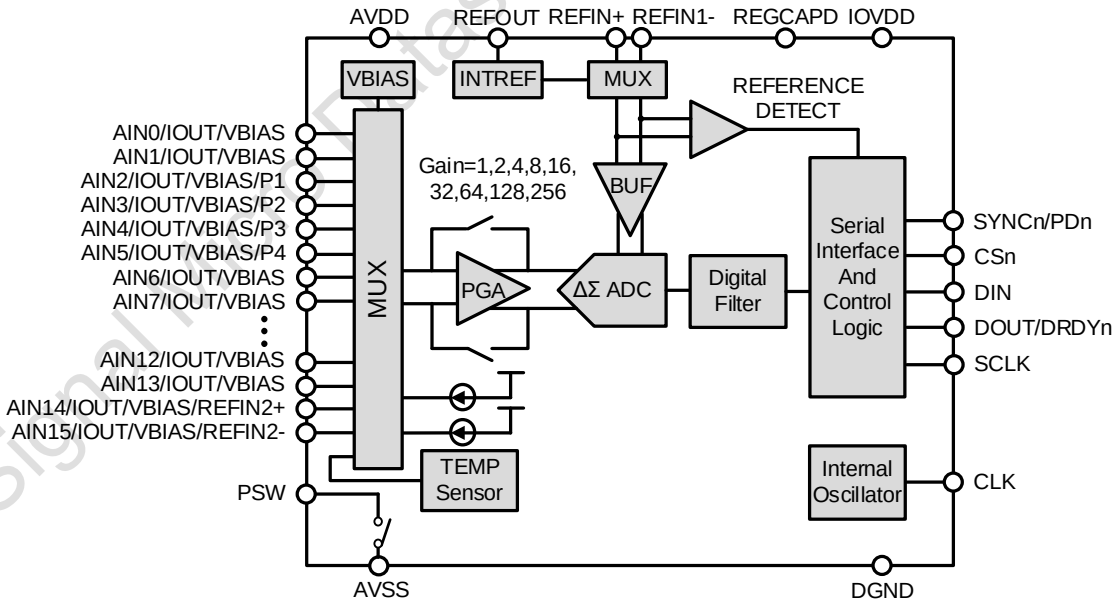
Programmable Gain: 1/2/4/8/16/32/64/128/256
Offset Drift: 5nV/°C (Gain=128)
Gain Drift: 1ppm/°C
2.5V Internal Reference with 5ppm/°C Drift
Integral Non-Linearity: 2ppm
Simultaneous 50Hz/60Hz Rejection at 25sps
8 Differential/15 Pseudo Differential Inputs
Automatic Channel Sequencer
Per Channel Configuration
Matched programmable Current Sources
Internal or External Clock
On-Chip Bias Voltage Generator
Low-Side Power Switch
General-Purpose Outputs
Multiple Filter Options: SINC4/SINC3/SINC1/POST_FILTER
Internal Temperature Sensor
Self and System Calibration
Burnout Current Sources
Parity Check
Power Supply
- **AVDD: 2.7V to 5.25V or ±1.5V to ±2.5V**
- **IOVDD: 2.7V to 5.25V**

Temperature range: -40°C to +125°C
Package: 32-lead LFCSP

APPLICATIONS

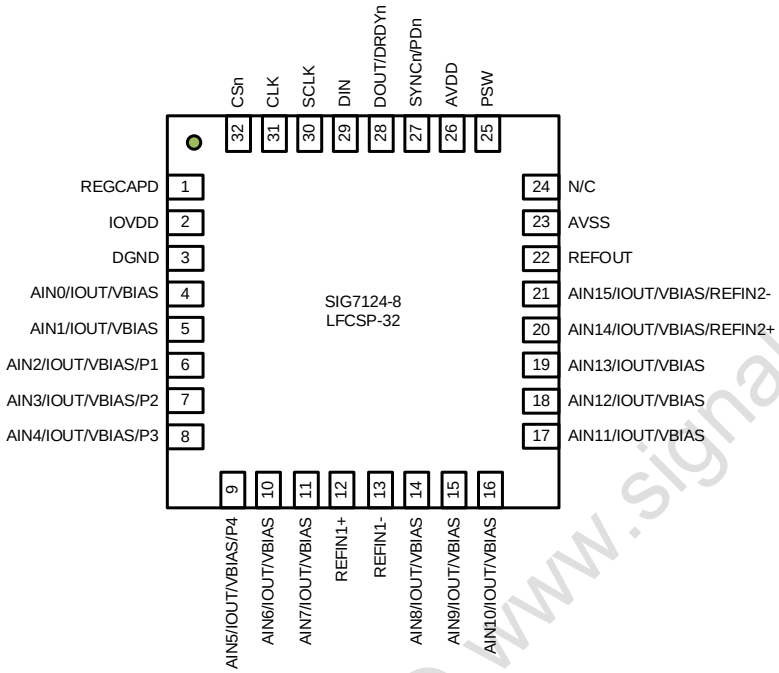
Temperature Measurement
Pressure Measurement
Industrial Process Control
Instrumentation
Smarter Transmitters

Function Block Diagram



PIN CONFIGURATION and DESCRIPTIONS

TOP VIEW (Not To Scale)



PIN		FUNCTION	DESCRIPTION
NO.	NAME		
1	REGCAPD	Digital	Digital LDO Regulator Output. Decouple this pin to DGND with a 0.1uF capacitor.
2	IOVDD	Digital	Digital power supply, 2.7V to 5.25V. IOVDD is independent of AVDD.
3	DGND	Digital	Digital ground reference point.
4	AIN0/IOUT/VBIAS	Analog Input/Output	Analog input channel 0/internal excitation current source/bias voltage.
5	AIN1/IOUT/VBIAS	Analog Input/Output	Analog input channel 1/internal excitation current source/bias voltage.
6	AIN2/IOUT/VBIAS/P1	Analog Input/Output	Analog input channel 2/internal excitation current source/bias voltage/general purpose output 1 between AVDD and AVSS.
7	AIN3/IOUT/VBIAS/P2	Analog Input/Output	Analog input channel 3/internal excitation current source/bias voltage/general purpose output 2 between AVDD and AVSS.
8	AIN4/IOUT/VBIAS/P3	Analog Input/Output	Analog input channel 4/internal excitation current source/bias voltage/general purpose output 3 between AVDD and AVSS.
9	AIN5/IOUT/VBIAS/P4	Analog Input/Output	Analog input channel 5/internal excitation current source/bias voltage/general purpose output 4 between AVDD and AVSS.
10	AIN6/IOUT/VBIAS	Analog Input/Output	Analog input channel 6/internal excitation current source/bias voltage.
11	AIN7/IOUT/VBIAS	Analog Input/Output	Analog input channel 7/internal excitation current source/bias voltage.
12	REFIN1+	Analog Input	Positive reference input.
13	REFIN1-	Analog Input	Negative reference input.
14	AIN8/IOUT/VBIAS	Analog Input/Output	Analog input channel 8/internal excitation current source/bias voltage.
15	AIN9/IOUT/VBIAS	Analog Input/Output	Analog input channel 9/internal excitation current source/bias voltage.
16	AIN10/IOUT/VBIAS	Analog Input/Output	Analog input channel 10/internal excitation current source/bias voltage.

17	AIN11/IOUT/VBIAS	Analog Input/Output	Analog input channel 11/internal excitation current source/bias voltage.
18	AIN12/IOUT/VBIAS	Analog Input/Output	Analog input channel 12/internal excitation current source/bias voltage.
19	AIN13/IOUT/VBIAS	Analog Input/Output	Analog input channel 13/internal excitation current source/bias voltage.
20	AIN14/IOUT/VBIAS/ REFIN2+	Analog Input/Output	Analog input channel 14/internal excitation current source/bias voltage/ positive reference input.
21	AIN15/IOUT/VBIAS/ REFIN2-	Analog Input/Output	Analog input channel 15/internal excitation current source/bias voltage/ negative reference input.
22	REFOUT	Analog	Internal Reference Output. Decouple this pin to AVSS with a 0.1uF capacitor.
23	AVSS	Analog	Negative analog power supply. AVSS can be taken below DGND to provide bipolar power supplies. For example, AVSS can be tied to –2.5V and AVDD can be tied to +2.5V, providing a ±2.5V dual supplies to the ADC.
24	NC	Digital	Not used.
25	PSW	Analog Input	Low-side Power switch to DGND.
26	AVDD	Analog	Positive analog power supply. 2.7V to 5.25V relative to DGND. AVDD is independent of IOVDD.
27	SYNCn_PDn	Digital Input	Synchronization control signal. While this pin is low, the digital filter is reset and DOUT pin is forced to high. The device starts a new conversion after this pin goes back to high. The device enters power-down if holding this pin low for longer than 0.83ms.
28	DOUT/DRDYn	Digital Output	Serial data output and data ready indicator.
29	DIN	Digital Input	Serial data input.
30	SCLK	Digital Input	Serial data clock.
31	CLK	Digital Input/Output	Master clock input or internal clock output depending on ADC_CTRL Register bits CLK_SEL[1:0].
32	CSn	Digital Input	Serial chip select. Active low.
Thermal Pad		–	Thermal power pad. Do not connect or only connect to AVSS.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKING OPTION
SIG7128	LFCSP-32	-40°C to +125°C	SIG7128-ICSP32-RL	Reel, 5000

SPECIFICATIONS

Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
Voltage	AVDD to AVSS	–0.3	6.5	V
	AVSS to DGND	–3	0.3	V
	IOVDD to DGND	–0.3	6.5	V
	Analog input	V_{AVSS} – 0.3	V_{AVDD} + 0.3	V
	Digital input	V_{DGND} – 0.3	V_{IOVDD} + 0.3	V
Current	Input current	–10	10	mA
Temperature	Junction (T_J)	–50	150	°C
	Storage (T_{stg})	-60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

SYMBOL	PARAMTER	CONDITION	VALUE	UNIT
HBM	Human-body Model	ANSI/ESDA/JEDEC JS-001	±4000	V
CDM	Charged-device model	JEDEC EIA/JS-002-2022	±2000	V

This integrated circuit can be damaged by ESD. Signal Micro recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Electrical Characteristics

Minimum/Maximum specifications apply from -40˚C to +125˚C. Typical specifications are at +25˚C. All specification are at V_{AVDD}=5.0V, V_{IOVDD}=3.3V, V_{DGND}=0V, V_{REF}=2.5V, f_{CLK}=4.9152MHz, data rate=10SPS, and PGA Gain=1, unless otherwise noted.

PARAMETER	TEST CONDITION OR NOTES	MIN(1)	TYP	MAX(1)	UNITS
ANALOG INPUTS					
Differential Input Voltage	$V_{IN} = V_{INP} – V_{INN}$	$–V_{REF}$/Gain		$+V_{REF}$/Gain	V
Absolute Input Voltage	Buffer Off	V_{AVSS} – 0.05		V_{AVDD} + 0.05	V
	Buffer On	V_{AVSS} + 0.2		V_{AVDD} – 0.2	
Common Mode Input Range	Buffer On	V_{AVSS} + 0.2 + $\lvert V_{INMAX}\rvert$·Gain/2		V_{AVDD} – 0.2 – $\lvert V_{INMAX}\rvert$·Gain/2	V
Absolute Input Current	Buffer off, Low Power		±10		nA
	Buffer off, Mid1 Power		±20		nA
	Buffer off, Mid2 Power		±40		nA
	Buffer off, Full Power		±80		nA
	Buffer On		±1		nA
SYSTEM PERFORMANCE					
PGA Gain		1/2/4/8/16/32/64/128/256			V/V
Resolution			24		Bits
Data Rate	Low Power Mode	1.17		2400	SPS
	Mid1 Power Mode	2.34		4800	SPS
	Mid2 Power Mode	4.67		9600	SPS
	Full Power Mode	9.34		19200	SPS
Noise		See Noise Table			
Integral Nonlinearity (INL)	Buffer Off		±10		ppm
	Buffer On		±2		ppm
Offset Error	Chop Off		±400/Gain		µV
	Chop On		±1		µV
Offset Drift vs. Temperature	All PGA gains		±400/Gain ± 2		nV/°C
Gain Error(2)	Gain = 1, 2, and 4	-0.005	±0.001	0.005	%
	Gain = 8, 16, and 32	-0.01	±0.004	0.01	
	Gain = 64, and 128	-0.025	±0.01	0.025	
Gain Drift vs. Temperature	All PGA gains	-3	±1	+3	ppm/°C
Normal Mode Rejection (NMRR)	f_{IN} = 50/60Hz, ±2%, data rate=10SPS		See Table 25		dB
Common Mode Rejection (CMRR)	f_{IN} = 50Hz, data rate = 1000SPS	95	120		dB
Power Supply Rejection (PSRR)	AVDD	85	105		dB
	IOVDD	90	110		dB
EXTERNAL REFERENCE INPUTS					
Differential Reference Voltage (V_{REF})	$V_{REF} = V_{REFP} – V_{REFN}$	0.5	2.5	V_{AVDD} + 0.1	V
Absolute Negative Reference Voltage (V_{REFN})		– 0.05		V_{REFP} – 0.5	V
Absolute Positive Reference Voltage (V_{REFP})		V_{REFN} + 0.5		V_{AVDD} + 0.05	V
Average Voltage Input Current	Low Power Mode		±30		nA
	Mid1 Power Mode		±70		nA
	Mid2 Power Mode		±140		nA
	Full Power Mode		±280		nA
INTERNAL VOLTAGE REFERENCE					
Reference Voltage			2.5		V
Initial Accuracy		-0.05%	±0.005%	+0.05%	
Temperature Drift		-20	±5	+20	ppm/°C

EXCITATION CURRENT SOURCES (IOUT1 and IOUT0)					
Output Current		50/100/250/500/750/1000			μA
Compliance Voltage(3)	IOUT<=250μA	V_{AVSS}		V_{AVDD} – 0.5	V
	IOUT=500μA	V_{AVSS}		V_{AVDD} – 0.6	
	IOUT=750μA	V_{AVSS}		V_{AVDD} – 0.7	
	IOUT=1000μA	V_{AVSS}		V_{AVDD} – 0.8	
Accuracy		-2%	±1%	+2%	
Current Mismatch IOUT1=IOUT2	50μA	-1.5%	±0.25%	+1.5%	
	100μA	-1.2%	±0.20%	+1.2%	
	250μA	-1.0%	±0.18%	+1.0%	
	500μA	-0.8%	±0.12%	+0.8%	
	750μA	-0.7%	±0.11%	+0.7%	
	1000μA	-0.6%	±0.1%	+0.6%	
Temperature Drift		-90	±20	+90	ppm/°C
Temperature Drift Mismatch		-30	±5	+30	ppm/°C
BURNOUT CURRENT SOURCES					
Current Setting			0.5/2/4		μA
ADC CLOCK					
External Clock	Frequency Range	1	4.9152	5.0	MHz
	Duty Cycle	40%		60%	
Internal Oscillator	Nominal Frequency		4.9152		MHz
	Accuracy	–3%	±0.5%	3%	
DIGITAL INPUT/OUTPUT					
High-level Output Voltage (V_{OH})	I_{OH} = 4mA	0.8·V_{IOVDD}			V
Low-level Output Voltage (V_{OL})	I_{OL} = –4mA			0.2· V_{IOVDD}	V
High-level Input Voltage (V_{IH})		0.7· V_{IOVDD}		V_{IOVDD}	V
Low-level Input Voltage (V_{IL})		V_{DGND}		0.3· V_{IOVDD}	V
Input Hysteresis			0.5		V
Input Leakage				±10	μA
POWER SUPPLY					
AVDD Voltage (V_{AVDD})		2.7		5.25	V
IOVDD Voltage (V_{IODD})		2.7		5.25	V
AVDD Current (I_{AVDD})	Buffer Off, Low Power		220	280	μA
	Buffer Off, Mid1 Power		340	420	μA
	Buffer Off, Mid2 Power		640	800	μA
	Buffer Off, Full Power		1400	1750	μA
	Buffer On, Low Power		430	500	μA
	Buffer On, Mid1 Power		700	900	μA
	Buffer On, Mid2 Power		1100	1400	μA
	Buffer On, Full Power		2300	2900	μA
	Sleep Mode		1		μA
	Power-down Mode		1		μA
IOVDD Current (I_{IOVDD})	Active Mode, Low Power		170	220	μA
	Active Mode, Mid1 Power		230	300	μA
	Active Mode, Mid2 Power		360	470	μA
	Active Mode, Full Power		600	780	μA
	Sleep Mode		22		μA
	Power-down Mode		1		μA

TEMPERATURE RANGE					
Specified temperature range		–40		125	°C
Operating temperature range		–50		125	°C
Storage temperature range		–60		150	°C

(1) Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
(2) MIN and MAX values listed for gain error are for +25˚C room temperature only.
(3) The IDAC current does not change by more than 0.01% from the nominal value when staying within the specified compliance voltage.

Timing Requirements: Serial Interface

Over the operating ambient temperature range and IOVDD = 2.7V to 5.25V, unless otherwise noted.

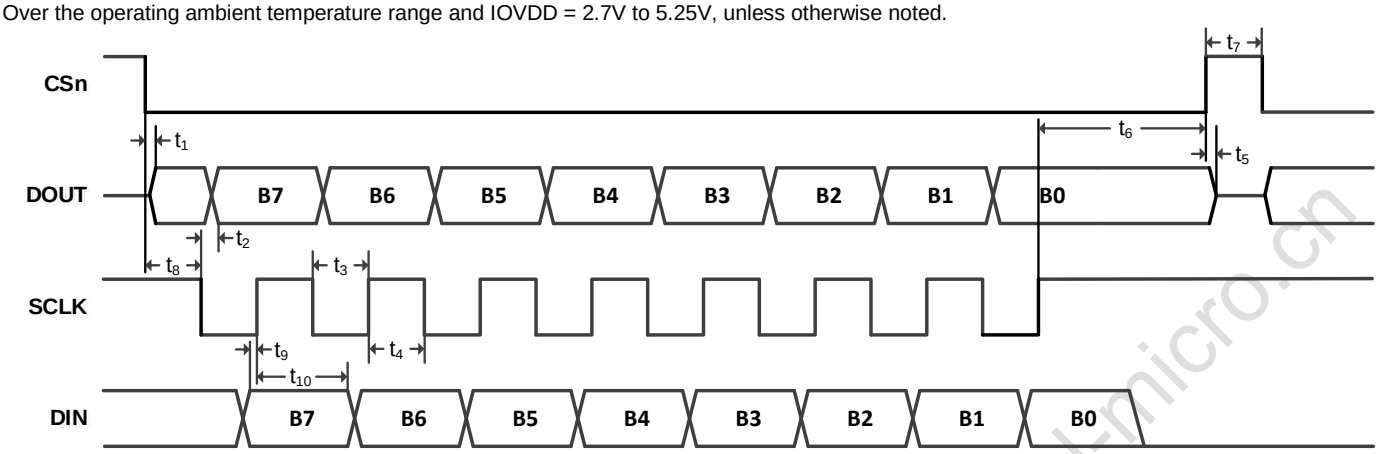


Figure 1. Serial Interface Timing Requirements

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_1	CSn falling edge to DOUT/DRDYn driven: propagation delay(1)		50	ns
t_2	SCLK falling edge to valid DOUT/DRDYn: propagation delay(1)		50	ns
t_3	SCLK low pulse width	100		ns
t_4	SCLK high pulse width	100		ns
	SCLK period	200	10^6	ns
t_5	CSn rising edge to DOUT high impedance: propagation delay		40	ns
t_6	Last SCLK rising edge to CSn rising edge: delay time	50		ns
t_7	CSn high pulse width	50		ns
t_8	CSn falling edge to first SCLK falling edge: setup time(2)	50		ns
t_9	Valid DIN to SCLK rising edge: setup time	50		ns
t_{10}	Valid DIN to SCLK rising edge: hold time	25		ns

(1) DOUT load = 20pF || 100kΩ to DGND.
(2) CSn can be tied low.

NOISE PERFORMANCE

The noise performance of the ADC is affected by PGA gain, data rate, and digital filter setting. The following tables show the rms noise and peak-to-peak noise for SINC4 and SINC3 filters and fast settling mode with chop disabled. The effective number of bits (ENOB) and noise-free bits are also listed according to Equation (1) and Equation (2):

$$\text{ENOB} = \log_2(2 \times V_{REF} / \text{Gain} / V_{RMS}) \quad (1)$$

$$\text{Noise Free Bits} = \log_2(2 \times V_{REF} / \text{Gain} / V_{p\text{-}p}) \quad (2)$$

The noise data listed in the table are typical and are generated from continuous ADC readings with differential input voltage of 0 V. With chop enabled, the resolution improves by 0.5 bits.

Full POWER MODE

SINC4 and Chop Disabled

Table 1. ADC Noise in μVRMS (μVPP) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	9.38	0.244(1.37)	0.152(0.897)	0.086(0.579)	0.045(0.270)	0.030(0.178)	0.022(0.142)	0.019(0.131)	0.018(0.117)	0.017(0.112)
1920	10	0.252(1.41)	0.157(0.926)	0.088(0.598)	0.047(0.278)	0.031(0.183)	0.023(0.147)	0.020(0.136)	0.018(0.121)	0.017(0.116)
960	20	0.356(2.00)	0.222(1.31)	0.125(0.846)	0.066(0.394)	0.044(0.259)	0.033(0.207)	0.028(0.192)	0.026(0.171)	0.024(0.163)
480	40	0.503(2.82)	0.313(1.85)	0.177(1.20)	0.093(0.557)	0.062(0.367)	0.046(0.293)	0.039(0.272)	0.037(0.242)	0.035(0.231)
384	50	0.563(3.15)	0.350(2.07)	0.198(1.34)	0.104(0.622)	0.070(0.410)	0.052(0.328)	0.044(0.304)	0.041(0.271)	0.039(0.258)
320	60	0.616(3.46)	0.384(2.27)	0.216(1.46)	0.114(0.682)	0.076(0.449)	0.056(0.359)	0.048(0.333)	0.045(0.297)	0.042(0.283)
240	80	0.712(3.99)	0.443(2.62)	0.250(1.69)	0.132(0.787)	0.088(0.518)	0.065(0.415)	0.056(0.384)	0.052(0.343)	0.049(0.327)
120	160	1.01(5.64)	0.627(3.70)	0.353(2.39)	0.187(1.11)	0.124(0.733)	0.092(0.587)	0.079(0.543)	0.074(0.485)	0.069(0.462)
60	320	1.42(7.98)	0.887(5.24)	0.500(3.38)	0.264(1.57)	0.176(1.04)	0.130(0.830)	0.111(0.768)	0.104(0.685)	0.098(0.654)
30	640	2.01(11.3)	1.25(7.41)	0.707(4.78)	0.373(2.23)	0.249(1.47)	0.184(1.17)	0.157(1.09)	0.147(0.969)	0.138(0.925)
15	1280	2.70(18.1)	1.59(9.95)	0.975(6.31)	0.528(3.30)	0.364(2.51)	0.278(2.02)	0.228(1.44)	0.209(1.47)	0.204(1.40)
8	2400	3.81(26.1)	2.13(15.7)	1.25(8.69)	0.715(5.16)	0.487(3.45)	0.362(2.54)	0.311(2.27)	0.287(2.02)	0.272(1.88)
4	4800	5.23(37.4)	3.22(23.8)	1.81(13.4)	1.05(6.91)	0.679(5.25)	0.516(3.61)	0.439(3.20)	0.414(3.06)	0.397(2.85)
2	9600	7.82(57.0)	4.73(35.5)	2.61(20.0)	1.51(11.2)	0.995(6.94)	0.728(5.69)	0.634(4.66)	0.574(4.59)	0.561(4.13)
1	19200	30.5(277)	15.7(206)	8.05(92.1)	4.12(36.6)	2.28(19.6)	1.36(11.6)	0.999(8.19)	0.851(6.42)	0.798(6.30)

Table 2. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	9.38	24.3(21.8)	24.0(21.4)	23.8(21.0)	23.7(21.1)	23.3(20.7)	22.7(20.1)	22.0(19.2)	21.1(18.3)	20.2(17.4)
1920	10	24.2(21.8)	23.9(21.4)	23.8(21.0)	23.7(21.1)	23.3(20.7)	22.7(20.0)	21.9(19.1)	21.0(18.3)	20.1(17.4)
960	20	23.7(21.3)	23.4(20.9)	23.3(20.5)	23.2(20.6)	22.8(20.2)	22.2(19.5)	21.4(18.6)	20.5(17.8)	19.6(16.9)
480	40	23.2(20.8)	22.9(20.4)	22.8(20.0)	22.7(20.1)	22.3(19.7)	21.7(19.0)	20.9(18.1)	20.0(17.3)	19.1(16.4)
384	50	23.1(20.6)	22.8(20.2)	22.6(19.8)	22.5(19.9)	22.1(19.5)	21.5(18.9)	20.8(18.0)	19.9(17.1)	18.9(16.2)
320	60	23.0(20.5)	22.6(20.1)	22.5(19.7)	22.4(19.8)	22.0(19.4)	21.4(18.7)	20.6(17.8)	19.7(17.0)	18.8(16.1)
240	80	22.7(20.3)	22.4(19.9)	22.3(19.5)	22.2(19.6)	21.8(19.2)	21.2(18.5)	20.4(17.6)	19.5(16.8)	18.6(15.9)
120	160	22.2(19.8)	21.9(19.4)	21.8(19.0)	21.7(19.1)	21.3(18.7)	20.7(18.0)	19.9(17.1)	19.0(16.3)	18.1(15.4)
60	320	21.7(19.3)	21.4(18.9)	21.3(18.5)	21.2(18.6)	20.8(18.2)	20.2(17.5)	19.4(16.6)	18.5(15.8)	17.6(14.9)
30	640	21.2(18.8)	20.9(18.4)	20.8(18.0)	20.7(18.1)	20.3(17.7)	19.7(17.0)	18.9(16.1)	18.0(15.3)	17.1(14.4)
15	1280	20.8(18.1)	20.6(17.9)	20.3(17.6)	20.2(17.5)	19.7(16.9)	19.1(16.2)	18.4(15.7)	17.5(14.7)	16.5(13.8)
8	2400	20.3(17.5)	20.2(17.3)	19.9(17.1)	19.7(16.9)	19.3(16.5)	18.7(15.9)	17.9(15.1)	17.1(14.2)	16.1(13.3)
4	4800	19.9(17.0)	19.6(16.7)	19.4(16.5)	19.2(16.5)	18.8(15.9)	18.2(15.4)	17.4(14.6)	16.5(13.6)	15.6(12.7)
2	9600	19.3(16.4)	19.0(16.1)	18.9(15.9)	18.7(15.8)	18.3(15.5)	17.7(14.7)	16.9(14.0)	16.1(13.1)	15.1(12.2)
1	19200	17.3(14.1)	17.3(13.6)	17.2(13.7)	17.2(14.1)	17.1(14.0)	16.8(13.7)	16.3(13.2)	15.5(12.6)	14.6(11.6)

Table 3. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 5 V, V_{REF} = 5 V, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	9.38	25.1(22.5)	25.0(22.3)	24.8(22.3)	24.7(22.0)	24.3(21.9)	23.8(21.1)	23.0(20.3)	22.1(19.4)	21.2(18.4)
1920	10	25.1(22.5)	24.9(22.2)	24.8(22.3)	24.6(22.0)	24.3(21.8)	23.8(21.1)	22.9(20.2)	22.1(19.3)	21.1(18.4)
960	20	24.6(22.0)	24.4(21.7)	24.3(21.8)	24.1(21.5)	23.8(21.3)	23.3(20.6)	22.4(19.7)	21.6(18.8)	20.6(17.9)
480	40	24.1(21.5)	23.9(21.2)	23.8(21.3)	23.6(21.0)	23.3(20.8)	22.8(20.1)	21.9(19.2)	21.1(18.3)	20.1(17.4)
384	50	23.9(21.3)	23.8(21.1)	23.6(21.1)	23.5(20.8)	23.1(20.7)	22.6(19.9)	21.8(19.1)	20.9(18.2)	20.0(17.2)
320	60	23.8(21.2)	23.6(21.0)	23.5(21.0)	23.4(20.7)	23.0(20.5)	22.5(19.8)	21.6(18.9)	20.8(18.0)	19.8(17.1)
240	80	23.6(21.0)	23.4(20.7)	23.3(20.8)	23.1(20.5)	22.8(20.3)	22.3(19.6)	21.4(18.7)	20.6(17.8)	19.6(16.9)
120	160	23.1(20.5)	22.9(20.2)	22.8(20.3)	22.6(20.0)	22.3(19.8)	21.8(19.1)	20.9(18.2)	20.1(17.3)	19.1(16.4)
60	320	22.6(20.0)	22.4(19.7)	22.3(19.8)	22.1(19.5)	21.8(19.3)	21.3(18.6)	20.4(17.7)	19.6(16.8)	18.6(15.9)
30	640	22.1(19.5)	21.9(19.2)	21.8(19.3)	21.6(19.0)	21.3(18.8)	20.8(18.1)	19.9(17.2)	19.1(16.3)	18.1(15.4)
15	1280	21.7(19.0)	21.5(18.9)	21.4(18.6)	21.2(18.5)	20.8(18.1)	20.2(17.3)	19.5(16.8)	18.7(16.0)	17.6(14.7)
8	2400	21.3(18.5)	21.0(18.2)	20.9(18.2)	20.7(18.0)	20.3(17.4)	19.8(17.0)	18.9(16.1)	18.1(15.3)	17.2(14.5)
4	4800	20.8(17.9)	20.5(17.6)	20.4(17.5)	20.2(17.3)	19.9(17.1)	19.3(16.4)	18.5(15.6)	17.6(14.8)	16.7(13.8)
2	9600	20.0(17.1)	19.9(16.9)	19.7(16.8)	19.5(16.5)	19.3(16.3)	18.7(15.8)	18.0(15.1)	17.1(14.1)	16.2(13.3)
1	19200	17.4(14.1)	17.4(13.9)	17.4(14.3)	17.4(14.1)	17.3(14.3)	17.2(14.0)	17.0(13.8)	16.4(13.4)	15.6(12.6)

SINC3 and Chop Disabled

Table 4. ADC Noise in μVRMS (μVPP) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	9.38	0.249(1.62)	0.153(1.01)	0.093(0.629)	0.050(0.315)	0.033(0.200)	0.024(0.149)	0.021(0.137)	0.019(0.131)	0.018(0.122)
1920	10	0.257(1.67)	0.158(1.04)	0.096(0.650)	0.051(0.325)	0.034(0.207)	0.025(0.154)	0.021(0.141)	0.020(0.136)	0.019(0.126)
960	20	0.363(2.36)	0.224(1.47)	0.136(0.919)	0.073(0.459)	0.048(0.292)	0.035(0.218)	0.030(0.200)	0.028(0.192)	0.027(0.178)
480	40	0.513(3.34)	0.317(2.08)	0.192(1.30)	0.103(0.650)	0.067(0.413)	0.050(0.308)	0.043(0.283)	0.040(0.272)	0.038(0.252)
384	50	0.574(3.74)	0.354(2.32)	0.215(1.45)	0.115(0.726)	0.075(0.462)	0.056(0.345)	0.048(0.316)	0.044(0.304)	0.043(0.281)
320	60	0.629(4.09)	0.388(2.55)	0.235(1.59)	0.126(0.796)	0.083(0.506)	0.061(0.378)	0.053(0.346)	0.048(0.333)	0.047(0.308)
240	80	0.726(4.73)	0.448(2.94)	0.271(1.84)	0.145(0.919)	0.095(0.584)	0.070(0.436)	0.061(0.400)	0.056(0.384)	0.054(0.356)
120	160	1.03(6.68)	0.633(4.16)	0.384(2.60)	0.205(1.30)	0.135(0.826)	0.100(0.617)	0.086(0.565)	0.079(0.543)	0.076(0.503)
60	320	1.45(9.45)	0.895(5.88)	0.543(3.68)	0.290(1.84)	0.191(1.17)	0.141(0.872)	0.121(0.799)	0.112(0.768)	0.108(0.711)
30	640	2.05(13.4)	1.27(8.32)	0.767(5.20)	0.411(2.60)	0.270(1.65)	0.199(1.23)	0.172(1.13)	0.158(1.09)	0.152(1.01)
15	1280	2.87(19.9)	1.82(14.1)	0.987(7.13)	0.569(3.56)	0.378(2.38)	0.284(1.69)	0.249(1.54)	0.228(1.48)	0.214(1.38)
8	2400	3.95(29.7)	2.44(14.8)	1.42(9.50)	0.778(5.12)	0.510(3.97)	0.391(2.68)	0.329(2.31)	0.311(2.13)	0.292(1.98)
4	4800	7.21(49.6)	4.09(29.4)	2.23(16.0)	1.24(9.21)	0.773(5.79)	0.575(4.32)	0.471(3.46)	0.438(2.95)	0.422(2.77)
2	9600	35.0(220)	18.0(105)	8.95(54.2)	4.57(27.5)	2.38(16.1)	1.33(9.28)	0.873(6.46)	0.672(5.00)	0.614(4.52)
1	19200	275(1590)	137(784)	68.6(386)	34.7(196)	17.3(105)	8.68(49.8)	4.41(27.9)	2.34(16.6)	1.37(9.87)

Table 5. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	9.38	24.3(21.6)	24.0(21.2)	23.7(20.9)	23.6(20.9)	23.2(20.6)	22.6(20.0)	21.8(19.1)	21.0(18.2)	20.0(17.3)
1920	10	24.2(21.5)	23.9(21.2)	23.6(20.9)	23.5(20.9)	23.1(20.5)	22.6(20.0)	21.8(19.1)	20.9(18.1)	20.0(17.2)
960	20	23.7(21.0)	23.4(20.7)	23.1(20.4)	23.0(20.4)	22.6(20.0)	22.1(19.5)	21.3(18.6)	20.4(17.6)	19.5(16.7)
480	40	23.2(20.5)	22.9(20.2)	22.6(19.9)	22.5(19.9)	22.1(19.5)	21.6(19.0)	20.8(18.1)	19.9(17.1)	19.0(16.2)
384	50	23.1(20.4)	22.8(20.0)	22.5(19.7)	22.4(19.7)	22.0(19.4)	21.4(18.8)	20.6(17.9)	19.8(17.0)	18.8(16.1)
320	60	22.9(20.2)	22.6(19.9)	22.3(19.6)	22.2(19.6)	21.9(19.2)	21.3(18.7)	20.5(17.8)	19.6(16.8)	18.7(16.0)
240	80	22.7(20.0)	22.4(19.7)	22.1(19.4)	22.0(19.4)	21.6(19.0)	21.1(18.5)	20.3(17.6)	19.4(16.6)	18.5(15.7)
120	160	22.2(19.5)	21.9(19.2)	21.6(18.9)	21.5(18.9)	21.1(18.5)	20.6(18.0)	19.8(17.1)	18.9(16.1)	18.0(15.2)
60	320	21.7(19.0)	21.4(18.7)	21.1(18.4)	21.0(18.4)	20.6(18.0)	20.1(17.5)	19.3(16.6)	18.4(15.6)	17.5(14.7)
30	640	21.2(18.5)	20.9(18.2)	20.6(17.9)	20.5(17.9)	20.1(17.5)	19.6(17.0)	18.8(16.1)	17.9(15.1)	17.0(14.2)
15	1280	20.7(17.9)	20.4(17.4)	20.3(17.4)	20.1(17.4)	19.7(17.0)	19.1(16.5)	18.3(15.6)	17.4(14.7)	16.5(13.8)
8	2400	20.3(17.4)	20.0(17.4)	19.7(17.0)	19.6(16.9)	19.2(16.3)	18.6(15.8)	17.9(15.0)	16.9(14.2)	16.0(13.3)
4	4800	19.4(16.6)	19.2(16.4)	19.1(16.3)	18.9(16.1)	18.6(15.7)	18.1(15.1)	17.3(14.5)	16.4(13.7)	15.5(12.8)
2	9600	17.1(14.5)	17.1(14.5)	17.1(14.5)	17.1(14.5)	17.0(14.2)	16.8(14.0)	16.4(13.6)	15.8(12.9)	15.0(12.1)
1	19200	14.1(11.6)	14.2(11.6)	14.2(11.7)	14.1(11.6)	14.1(11.5)	14.1(11.6)	14.1(11.5)	14.0(11.2)	13.8(11.0)

Table 6. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 5 V, V_{REF} = 5 V, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	9.38	25.1(22.4)	24.9(22.2)	24.7(22.1)	24.6(21.9)	24.2(21.7)	23.6(21.0)	22.9(20.2)	22.0(19.3)	21.1(18.4)
1920	10	25.0(22.4)	24.8(22.2)	24.7(22.0)	24.6(21.8)	24.2(21.6)	23.6(20.9)	22.9(20.1)	21.9(19.3)	21.0(18.3)
960	20	24.5(21.9)	24.3(21.7)	24.2(21.5)	24.1(21.3)	23.7(21.1)	23.1(20.4)	22.4(19.6)	21.4(18.8)	20.5(17.8)
480	40	24.0(21.4)	23.8(21.2)	23.7(21.0)	23.6(20.8)	23.2(20.6)	22.6(19.9)	21.9(19.1)	20.9(18.3)	20.0(17.3)
384	50	23.8(21.2)	23.6(21.0)	23.5(20.9)	23.4(20.7)	23.0(20.5)	22.4(19.8)	21.7(19.0)	20.8(18.1)	19.9(17.2)
320	60	23.7(21.1)	23.5(20.9)	23.4(20.8)	23.3(20.5)	22.9(20.4)	22.3(19.6)	21.6(18.9)	20.7(18.0)	19.8(17.0)
240	80	23.5(20.9)	23.3(20.7)	23.2(20.5)	23.1(20.3)	22.7(20.1)	22.1(19.4)	21.4(18.6)	20.4(17.8)	19.5(16.8)
120	160	23.0(20.4)	22.8(20.2)	22.7(20.0)	22.6(19.8)	22.2(19.6)	21.6(18.9)	20.9(18.1)	19.9(17.3)	19.0(16.3)
60	320	22.5(19.9)	22.3(19.7)	22.2(19.5)	22.1(19.3)	21.7(19.1)	21.1(18.4)	20.4(17.6)	19.4(16.8)	18.5(15.8)
30	640	22.0(19.4)	21.8(19.2)	21.7(19.0)	21.6(18.8)	21.2(18.6)	20.6(17.9)	19.9(17.1)	18.9(16.3)	18.0(15.3)
15	1280	21.6(18.8)	21.4(18.7)	22.3(21.0)	21.0(18.4)	20.7(17.9)	20.2(17.5)	19.3(16.3)	18.4(15.7)	17.6(14.9)
8	2400	21.2(18.2)	20.9(18.3)	20.8(17.9)	20.5(17.9)	20.2(17.2)	19.6(16.9)	18.9(16.1)	18.0(15.2)	17.1(14.3)
4	4800	19.9(17.2)	19.8(17.1)	19.7(17.0)	19.6(16.8)	19.4(16.6)	16.3(11.8)	18.4(15.6)	17.5(14.6)	16.6(13.6)
2	9600	17.2(14.6)	17.1(14.6)	17.1(14.5)	17.1(14.5)	17.1(14.5)	17.1(14.4)	16.9(14.2)	16.6(13.7)	15.9(13.1)
1	19200	14.1(11.6)	14.2(11.6)	14.2(11.7)	14.1(11.6)	14.1(11.6)	14.1(11.6)	14.1(11.6)	14.1(11.5)	14.6(11.5)

Post Filters, SINC3 and Chop Disabled

Table 7. ADC Noise in μVRMS (μVPP) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Data Rate (SPS)	PGA GAIN								
	1	2	4	8	16	32	64	128	256
16.67	0.562(2.97)	0.391(1.93)	0.213(0.891)	0.132(0.631)	0.073(0.316)	0.059(0.288)	0.042(0.176)	0.041(0.172)	0.038(0.169)
20	0.581(3.27)	0.439(2.08)	0.223(1.04)	0.131(0.520)	0.078(0.353)	0.062(0.339)	0.047(0.190)	0.045(0.195)	0.044(0.197)
25	0.727(3.56)	0.459(2.23)	0.229(1.19)	0.150(0.705)	0.086(0.408)	0.064(0.362)	0.049(0.237)	0.047(0.204)	0.045(0.203)
27.27	0.823(3.86)	0.497(2.38)	0.249(1.26)	0.149(0.742)	0.088(0.427)	0.070(0.371)	0.053(0.251)	0.048(0.213)	0.046(0.216)

Table 8. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Data Rate (SPS)	PGA GAIN								
	1	2	4	8	16	32	64	128	256
16.67	23.1(20.7)	22.6(20.3)	22.5(20.4)	22.2(19.9)	22.0(19.9)	21.3(19.1)	20.8(18.8)	19.9(17.8)	19.0(16.8)
20	23.0(20.5)	22.4(20.2)	22.4(20.2)	22.2(20.2)	21.9(19.8)	21.3(18.8)	20.7(18.6)	19.7(17.6)	18.8(16.6)
25	22.7(20.4)	22.4(20.1)	22.4(20.0)	22.0(19.8)	21.8(19.5)	21.2(18.7)	20.6(18.3)	19.7(17.5)	18.7(16.6)
27.27	22.5(20.3)	22.3(20.0)	22.3(19.9)	22.0(19.7)	21.8(19.5)	21.1(18.7)	20.5(18.3)	19.6(17.5)	18.7(16.5)

Fast Settling, Average=16, SINC4 and Chop Disabled

Table 9. ADC Noise in μVRMS (μVPP) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
384	3.125	0.184(1.11)	0.121(0.643)	0.067(0.371)	0.039(0.223)	0.023(0.107)	0.018(0.090)	0.013(0.081)	0.014(0.064)	0.012(0.062)
120	10	0.330(1.99)	0.216(1.15)	0.121(0.664)	0.069(0.398)	0.041(0.191)	0.032(0.162)	0.024(0.146)	0.025(0.115)	0.022(0.111)
24	50	0.737(4.45)	0.483(2.57)	0.270(1.48)	0.154(0.891)	0.091(0.427)	0.071(0.362)	0.054(0.326)	0.055(0.258)	0.050(0.248)
20	60	0.832(4.86)	0.531(2.67)	0.318(1.56)	0.169(0.742)	0.110(0.501)	0.076(0.473)	0.064(0.353)	0.058(0.281)	0.057(0.311)
2	600	2.66(16.0)	1.60(9.65)	0.905(5.57)	0.504(2.78)	0.338(2.17)	0.254(1.68)	0.210(1.31)	0.202(1.18)	0.203(1.13)
1	1200	3.93(26.7)	2.44(15.1)	1.23(8.46)	0.746(6.05)	0.493(3.17)	0.363(2.34)	0.301(2.15)	0.293(1.91)	0.281(1.75)

Table 10. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
384	3.125	24.7(22.1)	24.3(21.9)	24.1(21.7)	23.9(21.4)	23.7(21.5)	23.1(20.7)	22.5(19.9)	21.4(19.2)	20.6(18.3)
120	10	23.9(21.3)	23.5(21.1)	23.3(20.8)	23.1(20.6)	22.9(20.6)	22.2(19.9)	21.6(19.0)	20.6(18.4)	19.7(17.4)
24	50	22.7(20.1)	22.3(19.9)	22.1(19.7)	21.9(19.4)	21.7(19.5)	21.1(18.7)	20.5(17.9)	19.4(17.2)	18.6(16.3)
20	60	22.5(20.0)	22.2(19.8)	21.9(19.6)	21.8(19.7)	21.4(19.3)	21.0(18.3)	20.2(17.8)	19.4(17.1)	18.4(15.9)
2	600	20.8(18.3)	20.6(18.0)	20.4(17.8)	20.2(17.8)	19.8(17.1)	19.2(16.5)	18.5(15.9)	17.6(15.0)	16.6(14.1)
1	1200	20.3(17.5)	20.0(17.3)	20.0(17.2)	19.7(16.7)	19.3(16.6)	18.7(16.0)	18.0(15.1)	17.0(14.3)	16.1(13.4)

Fast Settling, Average=16, SINC3 and Chop Disabled

Table 11. ADC Noise in μVRMS (μVPP) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
384	3.125	0.192(0.817)	0.123(0.594)	0.069(0.334)	0.040(0.204)	0.025(0.135)	0.019(0.102)	0.016(0.080)	0.014(0.071)	0.014(0.061)
120	10	0.343(1.46)	0.220(1.06)	0.123(0.598)	0.072(0.365)	0.044(0.241)	0.033(0.183)	0.029(0.143)	0.026(0.127)	0.024(0.110)
24	50	0.767(3.27)	0.493(2.38)	0.275(1.34)	0.161(0.817)	0.099(0.538)	0.074(0.408)	0.064(0.320)	0.058(0.285)	0.054(0.246)
20	60	0.866(4.16)	0.545(2.52)	0.337(1.86)	0.173(0.965)	0.114(0.538)	0.077(0.408)	0.071(0.353)	0.069(0.311)	0.064(0.281)
2	600	3.30(22.6)	1.89(11.9)	1.02(5.94)	0.574(3.12)	0.367(2.60)	0.268(1.58)	0.222(1.37)	0.197(1.32)	0.202(1.16)
1	1200	14.4(83.2)	7.16(47.5)	3.86(20.8)	1.83(11.9)	0.984(5.20)	0.489(3.34)	0.385(2.60)	0.316(1.96)	0.281(1.82)

Table 12. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
384	3.125	24.6(22.5)	24.3(22.0)	24.1(21.8)	23.9(21.5)	23.6(21.1)	23.0(20.5)	22.2(19.9)	21.4(19.1)	20.5(18.3)
120	10	23.8(21.7)	23.4(21.2)	23.3(21.0)	23.1(20.7)	22.7(20.3)	22.2(19.7)	21.4(19.1)	20.5(18.2)	19.6(17.4)
24	50	22.6(20.5)	22.3(20.0)	22.1(19.8)	21.9(19.5)	21.6(19.1)	21.0(18.5)	20.2(17.9)	19.4(17.1)	18.5(16.3)
20	60	22.5(20.2)	22.1(19.9)	21.8(19.4)	21.8(19.3)	21.4(19.1)	20.9(18.5)	20.1(17.8)	19.1(16.9)	18.2(16.1)
2	600	20.5(17.8)	20.3(17.7)	20.2(17.7)	20.1(17.6)	19.7(16.9)	19.2(16.6)	18.4(15.8)	17.6(14.9)	16.6(14.0)
1	1200	18.4(15.9)	18.4(15.7)	18.3(15.9)	18.4(15.7)	18.3(15.9)	18.3(15.5)	17.6(14.9)	16.9(14.3)	16.1(13.4)

MID2 POWER MODE

SINC4 and Chop Disabled

Table 13. ADC Noise in μVRMS (μVPP) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	4.69	0.227(1.22)	0.155(0.827)	0.081(0.494)	0.051(0.324)	0.028(0.180)	0.021(0.112)	0.017(0.103)	0.017(0.100)	0.016(0.092)
1920	5	0.234(1.26)	0.160(0.854)	0.084(0.510)	0.053(0.334)	0.029(0.186)	0.022(0.116)	0.018(0.107)	0.018(0.103)	0.017(0.095)
960	10	0.331(1.79)	0.226(1.21)	0.118(0.722)	0.075(0.473)	0.041(0.263)	0.031(0.164)	0.025(0.151)	0.025(0.146)	0.024(0.134)
480	20	0.469(2.52)	0.319(1.71)	0.167(1.02)	0.106(0.668)	0.057(0.371)	0.044(0.232)	0.036(0.213)	0.035(0.206)	0.033(0.190)
240	40	0.663(3.57)	0.452(2.42)	0.237(1.44)	0.150(0.945)	0.081(0.525)	0.062(0.328)	0.051(0.302)	0.050(0.291)	0.047(0.268)
192	50	0.741(3.99)	0.505(2.70)	0.265(1.61)	0.167(1.06)	0.091(0.587)	0.070(0.367)	0.057(0.338)	0.055(0.325)	0.053(0.300)
160	60	0.812(4.37)	0.553(2.96)	0.290(1.77)	0.183(1.16)	0.099(0.643)	0.076(0.402)	0.062(0.370)	0.061(0.356)	0.058(0.328)
120	80	0.938(5.05)	0.639(3.42)	0.335(2.04)	0.212(1.34)	0.115(0.742)	0.088(0.464)	0.072(0.427)	0.070(0.412)	0.067(0.379)
60	160	1.33(7.14)	0.904(4.83)	0.474(2.89)	0.299(1.89)	0.162(1.05)	0.125(0.656)	0.102(0.604)	0.099(0.582)	0.094(0.536)
30	320	1.88(10.1)	1.28(6.83)	0.670(4.08)	0.423(2.67)	0.229(1.48)	0.177(0.928)	0.144(0.854)	0.140(0.823)	0.133(0.759)
16	600	2.45(14.3)	1.61(10.1)	0.875(5.94)	0.493(2.97)	0.334(1.93)	0.243(1.74)	0.198(1.16)	0.194(1.27)	0.189(1.11)
8	1200	3.87(25.5)	2.18(13.7)	1.34(8.02)	0.749(4.83)	0.457(2.73)	0.345(2.47)	0.279(1.86)	0.269(1.57)	0.260(1.68)
4	2400	5.27(37.1)	3.32(24.5)	1.82(11.6)	1.05(7.76)	0.657(5.05)	0.499(3.57)	0.426(3.17)	0.376(2.70)	0.364(2.65)
2	4800	7.83(65.0)	4.81(33.4)	2.63(18.0)	1.51(10.4)	0.949(6.87)	0.694(4.73)	0.591(4.35)	0.539(4.07)	0.502(3.78)
1	9600	30.2(324)	15.9(127)	8.05(83.5)	4.15(44.8)	2.22(17.8)	1.30(10.1)	0.923(6.81)	0.785(6.11)	0.742(6.31)

Table 14. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	4.69	24.4(22.0)	23.9(21.5)	23.9(21.3)	23.5(20.9)	23.4(20.7)	22.8(20.4)	22.1(19.5)	21.1(18.6)	20.2(17.7)
1920	5	24.3(21.9)	23.9(21.5)	23.8(21.2)	23.5(20.8)	23.4(20.7)	22.8(20.4)	22.1(19.5)	21.1(18.5)	20.2(17.7)
960	10	23.8(21.4)	23.4(21.0)	23.3(20.7)	23.0(20.3)	22.9(20.2)	22.3(19.9)	21.6(19.0)	20.6(18.0)	19.7(17.2)
480	20	23.3(20.9)	22.9(20.5)	22.8(20.2)	22.5(19.8)	22.4(19.7)	21.8(19.4)	21.1(18.5)	20.1(17.5)	19.2(16.7)
240	40	22.8(20.4)	22.4(20.0)	22.3(19.7)	22.0(19.3)	21.9(19.2)	21.3(18.9)	20.6(18.0)	19.6(17.0)	18.7(16.2)
192	50	22.7(20.3)	22.2(19.8)	22.2(19.6)	21.8(19.2)	21.7(19.0)	21.1(18.7)	20.4(17.8)	19.4(16.9)	18.5(16.0)
160	60	22.6(20.1)	22.1(19.7)	22.0(19.4)	21.7(19.0)	21.6(18.9)	21.0(18.6)	20.3(17.7)	19.3(16.7)	18.4(15.9)
120	80	22.3(19.9)	21.9(19.5)	21.8(19.2)	21.5(18.8)	21.4(18.7)	20.8(18.4)	20.1(17.5)	19.1(16.5)	18.2(15.7)
60	160	21.8(19.4)	21.4(19.0)	21.3(18.7)	21.0(18.3)	20.9(18.2)	20.3(17.9)	19.6(17.0)	18.6(16.0)	17.7(15.2)
30	320	21.3(18.9)	20.9(18.5)	20.8(18.2)	20.5(17.8)	20.4(17.7)	19.8(17.4)	19.1(16.5)	18.1(15.5)	17.2(14.7)
16	600	21.0(18.4)	20.6(17.9)	20.4(17.7)	20.3(17.7)	19.8(17.3)	19.3(16.5)	18.6(16.0)	17.6(14.9)	16.7(14.1)
8	1200	20.3(17.6)	20.1(17.5)	19.8(17.3)	19.7(17.0)	19.4(16.8)	18.8(15.9)	18.1(15.4)	17.1(14.6)	16.2(13.5)
4	2400	19.9(17.0)	19.5(16.6)	19.4(16.7)	19.2(16.3)	18.9(15.9)	18.3(15.4)	17.5(14.6)	16.7(13.8)	15.7(12.8)
2	4800	19.3(16.2)	19.0(16.2)	18.9(16.1)	18.7(15.9)	18.3(15.5)	17.8(15.0)	17.0(14.1)	16.1(13.2)	15.2(12.3)
1	9600	17.3(13.9)	17.3(14.3)	17.2(13.9)	17.2(13.8)	17.1(14.1)	16.9(13.9)	16.4(13.5)	15.6(12.6)	14.7(11.6)

Table 15. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 5 V, V_{REF} = 5 V, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	4.69	25.3(22.7)	24.9(22.5)	24.8(22.4)	24.7(22.2)	24.3(21.8)	23.8(21.4)	23.2(20.7)	22.3(19.9)	21.4(19.0)
1920	5	25.2(22.7)	24.9(22.4)	24.8(22.3)	24.6(22.1)	24.2(21.8)	23.8(21.4)	23.1(20.6)	22.2(19.9)	21.3(18.9)
960	10	24.7(22.2)	24.4(21.9)	24.3(21.8)	24.1(21.6)	23.7(21.3)	23.3(20.9)	22.6(20.1)	21.7(19.4)	20.8(18.4)
480	20	24.2(21.7)	23.9(21.4)	23.8(21.3)	23.6(21.1)	23.2(20.8)	22.8(20.4)	22.1(19.6)	21.2(18.9)	20.3(17.9)
240	40	23.7(21.2)	23.4(20.9)	23.3(20.8)	23.1(20.6)	22.7(20.3)	22.3(19.9)	21.6(19.1)	20.7(18.4)	19.8(17.4)
192	50	23.6(21.0)	23.2(20.8)	23.1(20.7)	22.9(20.5)	22.6(20.1)	22.1(19.7)	21.5(19.0)	20.6(18.2)	19.6(17.3)
160	60	23.4(20.9)	23.1(20.6)	23.0(20.5)	22.8(20.4)	22.4(20.0)	22.0(19.6)	21.3(18.8)	20.4(18.1)	19.5(17.2)
120	80	23.2(20.7)	22.9(20.4)	22.8(20.3)	22.6(20.1)	22.2(19.8)	21.8(19.4)	21.1(18.6)	20.2(17.9)	19.3(16.9)
60	160	22.7(20.2)	22.4(19.9)	22.3(19.8)	22.1(19.6)	21.7(19.3)	21.3(18.9)	20.6(18.1)	19.7(17.4)	18.8(16.4)
30	320	22.2(19.7)	21.9(19.4)	21.8(19.3)	21.6(19.1)	21.2(18.8)	20.8(18.4)	20.1(17.6)	19.2(16.9)	18.3(15.9)
16	600	21.8(19.3)	21.5(18.9)	21.3(18.9)	21.2(18.5)	20.8(18.1)	20.3(17.7)	19.6(16.8)	18.7(16.1)	17.9(15.2)
8	1200	21.3(18.6)	21.0(18.5)	20.8(18.2)	20.7(17.9)	20.4(17.7)	19.8(17.0)	19.1(16.4)	18.3(15.6)	17.3(14.8)
4	2400	20.9(18.0)	20.5(17.7)	20.4(17.8)	20.2(17.4)	19.8(17.0)	19.3(16.5)	18.6(15.9)	17.7(14.7)	16.8(13.9)
2	4800	20.1(17.2)	19.8(17.0)	19.7(16.8)	19.5(16.5)	19.3(16.3)	18.8(15.9)	18.1(15.1)	17.2(14.4)	16.3(13.3)
1	9600	17.4(14.1)	17.4(14.3)	17.4(14.2)	17.4(14.2)	17.3(14.0)	17.2(14.0)	17.0(13.9)	16.5(13.6)	15.7(12.8)

SINC3 and Chop Disabled

Table 16. ADC Noise in μVRMS (μVPP) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	4.69	0.248(1.44)	0.161(0.881)	0.089(0.503)	0.055(0.330)	0.031(0.191)	0.023(0.119)	0.020(0.117)	0.018(0.113)	0.017(0.096)
1920	5	0.256(1.48)	0.166(0.910)	0.092(0.520)	0.057(0.341)	0.032(0.197)	0.024(0.123)	0.020(0.121)	0.019(0.116)	0.017(0.099)
960	10	0.363(2.10)	0.235(1.29)	0.130(0.735)	0.081(0.482)	0.045(0.278)	0.034(0.174)	0.029(0.171)	0.027(0.164)	0.025(0.141)
480	20	0.513(2.97)	0.333(1.82)	0.184(1.04)	0.114(0.681)	0.063(0.393)	0.048(0.246)	0.041(0.241)	0.038(0.233)	0.035(0.199)
240	40	0.725(4.20)	0.470(2.57)	0.260(1.47)	0.162(0.963)	0.090(0.556)	0.067(0.348)	0.057(0.341)	0.053(0.329)	0.049(0.281)
192	50	0.811(4.70)	0.526(2.88)	0.291(1.64)	0.181(1.08)	0.100(0.622)	0.075(0.389)	0.064(0.382)	0.060(0.368)	0.055(0.315)
160	60	0.888(5.14)	0.576(3.15)	0.318(1.80)	0.198(1.18)	0.110(0.681)	0.083(0.426)	0.070(0.418)	0.065(0.403)	0.060(0.345)
120	80	1.03(5.94)	0.665(3.64)	0.368(2.08)	0.229(1.36)	0.127(0.787)	0.095(0.492)	0.081(0.483)	0.075(0.465)	0.070(0.398)
60	160	1.45(8.40)	0.940(5.15)	0.520(2.94)	0.324(1.93)	0.179(1.11)	0.135(0.696)	0.115(0.683)	0.106(0.658)	0.099(0.563)
30	320	2.05(11.9)	1.33(7.28)	0.735(4.16)	0.458(2.72)	0.254(1.57)	0.191(0.984)	0.162(0.965)	0.151(0.930)	0.139(0.796)
16	600	3.04(21.4)	1.71(10.4)	0.978(5.64)	0.582(3.86)	0.352(2.19)	0.263(1.57)	0.215(1.25)	0.206(1.31)	0.199(1.15)
8	1200	3.98(24.7)	2.38(15.3)	1.35(8.76)	0.799(5.53)	0.513(3.17)	0.364(2.56)	0.307(1.98)	0.280(1.92)	0.272(1.81)
4	2400	7.12(51.1)	4.02(26.7)	2.23(16.2)	1.24(8.87)	0.747(5.01)	0.545(3.71)	0.434(3.32)	0.417(2.99)	0.394(2.81)
2	4800	35.6(211)	18.4(104)	8.97(52.7)	4.55(27.1)	2.34(16.0)	1.32(8.63)	0.826(5.94)	0.638(4.63)	0.570(4.26)
1	9600	280(1570)	139(808)	68.0(386)	34.0(193)	17.2(101)	8.56(50.5)	4.45(26.0)	2.27(14.3)	1.34(8.85)

Table 17. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	4.69	24.3(21.7)	23.9(21.4)	23.7(21.2)	23.4(20.9)	23.3(20.6)	22.7(20.3)	21.9(19.4)	21.0(18.4)	20.1(17.6)
1920	5	24.2(21.7)	23.8(21.4)	23.7(21.2)	23.4(20.8)	23.2(20.6)	22.6(20.3)	21.9(19.3)	21.0(18.4)	20.1(17.6)
960	10	23.7(21.2)	23.3(20.9)	23.2(20.7)	22.9(20.3)	22.7(20.1)	22.1(19.8)	21.4(18.8)	20.5(17.9)	19.6(17.1)
480	20	23.2(20.7)	22.8(20.4)	22.7(20.2)	22.4(19.8)	22.2(19.6)	21.6(19.3)	20.9(18.3)	20.0(17.4)	19.1(16.6)
240	40	22.7(20.2)	22.3(19.9)	22.2(19.7)	21.9(19.3)	21.7(19.1)	21.1(18.8)	20.4(17.8)	19.5(16.9)	18.6(16.1)
192	50	22.6(20.0)	22.2(19.7)	22.0(19.5)	21.7(19.1)	21.6(18.9)	21.0(18.6)	20.2(17.6)	19.3(16.7)	18.4(15.9)
160	60	22.4(19.9)	22.0(19.6)	21.9(19.4)	21.6(19.0)	21.4(18.8)	20.9(18.5)	20.1(17.5)	19.2(16.6)	18.3(15.8)
120	80	22.2(19.7)	21.8(19.4)	21.7(19.2)	21.4(18.8)	21.2(18.6)	20.6(18.3)	19.9(17.3)	19.0(16.4)	18.1(15.6)
60	160	21.7(19.2)	21.3(18.9)	21.2(18.7)	20.9(18.3)	20.7(18.1)	20.1(17.8)	19.4(16.8)	18.5(15.9)	17.6(15.1)
30	320	21.2(18.7)	20.8(18.4)	20.7(18.2)	20.4(17.8)	20.2(17.6)	19.6(17.3)	18.9(16.3)	18.0(15.4)	17.1(14.6)
16	600	20.6(17.8)	20.5(17.9)	20.3(17.8)	20.0(17.3)	19.8(17.1)	19.2(16.6)	18.5(15.9)	17.5(14.9)	16.6(14.0)
8	1200	20.3(17.6)	20.0(17.3)	19.8(17.1)	19.6(16.8)	19.2(16.6)	18.7(15.9)	18.0(15.3)	17.1(14.3)	16.1(13.4)
4	2400	19.4(16.6)	19.2(16.5)	19.1(16.2)	18.9(16.1)	18.7(15.9)	18.1(15.4)	17.5(14.5)	16.5(13.7)	15.6(12.8)
2	4800	17.1(14.5)	17.0(14.6)	17.1(14.5)	17.1(14.5)	17.0(14.3)	16.9(14.1)	16.5(13.7)	15.9(13.0)	15.1(12.2)
1	9600	14.1(11.6)	14.1(11.6)	14.2(11.7)	14.2(11.7)	14.1(11.6)	14.2(11.6)	14.1(11.6)	14.1(11.4)	13.8(11.1)

Table 18. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 5 V, V_{REF} = 5 V, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	4.69	25.1(22.3)	24.8(22.3)	24.6(22.2)	24.4(22.0)	24.2(21.6)	23.7(21.1)	23.0(20.4)	22.2(19.6)	21.2(18.7)
1920	5	25.0(22.2)	24.8(22.3)	24.6(22.2)	24.4(21.9)	24.2(21.5)	23.6(21.1)	22.9(20.4)	22.1(19.5)	21.2(18.6)
960	10	24.5(21.7)	24.3(21.8)	24.1(21.7)	23.9(21.4)	23.7(21.0)	23.1(20.6)	22.4(19.9)	21.6(19.0)	20.7(18.1)
480	20	24.0(21.2)	23.8(21.3)	23.6(21.2)	23.4(20.9)	23.2(20.5)	22.6(20.1)	21.9(19.4)	21.1(18.5)	20.2(17.6)
240	40	23.5(20.7)	23.3(20.8)	23.1(20.7)	22.9(20.4)	22.7(20.0)	22.1(19.6)	21.4(18.9)	20.6(18.0)	19.7(17.1)
192	50	23.4(20.6)	23.1(20.6)	22.9(20.5)	22.7(20.3)	22.5(19.9)	22.0(19.4)	21.3(18.7)	20.4(17.9)	19.5(16.9)
160	60	23.3(20.5)	23.0(20.5)	22.8(20.4)	22.6(20.1)	22.4(19.8)	21.8(19.3)	21.1(18.6)	20.3(17.7)	19.4(16.8)
120	80	23.0(20.2)	22.8(20.3)	22.6(20.2)	22.4(19.9)	22.2(19.5)	21.6(19.1)	20.9(18.4)	20.1(17.5)	19.2(16.6)
60	160	22.5(19.7)	22.3(19.8)	22.1(19.7)	21.9(19.4)	21.7(19.0)	21.1(18.6)	20.4(17.9)	19.6(17.0)	18.7(16.1)
30	320	22.0(19.2)	21.8(19.3)	21.6(19.2)	21.4(18.9)	21.2(18.5)	20.6(18.1)	19.9(17.4)	19.1(16.5)	18.2(15.6)
16	600	21.6(19.1)	21.3(18.8)	21.2(18.4)	21.1(18.4)	20.7(18.2)	20.3(17.9)	19.4(16.7)	18.6(15.9)	17.7(14.8)
8	1200	21.2(18.6)	20.8(18.1)	20.8(18.1)	20.5(17.7)	20.2(17.6)	19.7(17.0)	19.0(16.3)	18.1(15.5)	17.2(14.5)
4	2400	19.9(17.2)	19.8(16.9)	19.7(17.0)	19.6(16.9)	19.4(16.7)	19.1(16.2)	18.4(15.6)	17.6(14.7)	16.6(13.9)
2	4800	17.1(14.6)	17.1(14.7)	17.1(14.6)	17.1(14.6)	17.1(14.6)	17.1(14.5)	16.9(14.3)	16.6(13.8)	16.0(13.2)
1	9600	14.1(11.6)	14.1(11.7)	14.1(11.6)	14.2(11.6)	14.1(11.6)	14.1(11.7)	14.2(11.6)	14.1(11.6)	14.1(11.4)

Post Filters, SINC3 and Chop Disabled

Table 19. ADC Noise in µVRMS (µVPP) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Data Rate (SPS)	PGA GAIN								
	1	2	4	8	16	32	64	128	256
16.67	0.815(3.45)	0.510(2.23)	0.305(1.28)	0.161(0.706)	0.098(0.408)	0.080(0.371)	0.059(0.246)	0.053(0.228)	0.053(0.214)
20	0.839(3.56)	0.556(2.38)	0.311(1.34)	0.164(0.749)	0.100(0.481)	0.082(0.381)	0.061(0.292)	0.058(0.263)	0.055(0.247)
25	0.961(4.46)	0.584(2.82)	0.325(1.48)	0.191(0.891)	0.107(0.557)	0.087(0.408)	0.071(0.320)	0.062(0.296)	0.059(0.290)
27.27	1.03(5.05)	0.659(3.27)	0.361(1.63)	0.203(1.00)	0.120(0.631)	0.093(0.455)	0.076(0.353)	0.067(0.318)	0.061(0.302)

Table 20. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Data Rate (SPS)	PGA GAIN								
	1	2	4	8	16	32	64	128	256
16.67	22.5(20.5)	22.2(20.1)	22.0(19.9)	21.9(19.8)	21.6(19.5)	20.9(18.7)	20.3(18.3)	19.5(17.4)	18.5(16.5)
20	22.5(20.4)	22.1(20.0)	21.9(19.8)	21.9(19.7)	21.6(19.3)	20.9(18.6)	20.3(18.0)	19.4(17.2)	18.4(16.3)
25	22.3(20.1)	22.0(19.8)	21.9(19.7)	21.6(19.4)	21.5(19.1)	20.8(18.5)	20.1(17.9)	19.3(17.0)	18.3(16.0)
27.27	22.2(19.9)	21.9(19.5)	21.7(19.5)	21.6(19.3)	21.3(18.9)	20.7(18.4)	20.0(17.8)	19.1(16.9)	18.3(16.0)

Fast Settling, Average=16, SINC4 and Chop Disabled

Table 21. ADC Noise in µVRMS (µVPP) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
192	3.125	0.289(1.49)	0.161(0.804)	0.094(0.463)	0.053(0.251)	0.031(0.158)	0.024(0.119)	0.020(0.099)	0.019(0.096)	0.019(0.095)
30	10	0.518(2.66)	0.288(1.44)	0.168(0.829)	0.095(0.448)	0.055(0.282)	0.042(0.213)	0.035(0.177)	0.035(0.171)	0.034(0.169)
12	50	1.16(5.95)	0.643(3.22)	0.375(1.85)	0.212(1.00)	0.124(0.631)	0.094(0.476)	0.079(0.395)	0.078(0.383)	0.076(0.378)
10	60	1.28(6.53)	0.739(3.86)	0.425(2.23)	0.243(1.19)	0.152(0.798)	0.104(0.585)	0.085(0.427)	0.081(0.411)	0.078(0.398)
2	300	2.67(14.6)	1.60(11.9)	0.917(5.05)	0.522(3.12)	0.317(1.91)	0.224(1.50)	0.197(1.28)	0.190(1.15)	0.181(0.991)
1	600	4.00(27.6)	2.42(13.7)	1.30(8.32)	0.724(4.31)	0.461(2.99)	0.336(2.00)	0.291(1.75)	0.268(1.58)	0.252(1.57)

Table 22. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
192	3.125	24.0(21.7)	23.9(21.6)	23.7(21.4)	23.5(21.3)	23.3(20.9)	22.7(20.3)	21.9(19.6)	20.9(18.6)	20.0(17.7)
30	10	23.2(20.8)	23.1(20.7)	22.8(20.5)	22.7(20.4)	22.4(20.1)	21.8(19.5)	21.1(18.8)	20.1(17.8)	19.1(16.8)
12	50	22.0(19.7)	21.9(19.6)	21.7(19.4)	21.5(19.3)	21.3(18.9)	20.7(18.3)	19.9(17.6)	18.9(16.6)	18.0(15.7)
10	60	21.9(19.5)	21.7(19.3)	21.5(19.1)	21.3(19.0)	21.0(18.6)	20.5(18.0)	19.8(17.5)	18.9(16.5)	17.9(15.6)
2	300	20.8(18.4)	20.6(17.7)	20.4(17.9)	20.2(17.6)	19.9(17.3)	19.4(16.7)	18.6(15.9)	17.6(15.1)	16.7(14.3)
1	600	20.3(17.5)	20.0(17.5)	19.9(17.2)	19.7(17.1)	19.4(16.7)	18.8(16.3)	18.0(15.4)	17.2(14.6)	16.2(13.6)

Fast Settling, Average=16, SINC3 and Chop Disabled

Table 23. ADC Noise in µVRMS (µVPP) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
192	3.125	0.305(1.63)	0.171(0.854)	0.096(0.493)	0.055(0.232)	0.035(0.153)	0.024(0.118)	0.021(0.106)	0.020(0.098)	0.019(0.097)
30	10	0.546(2.92)	0.306(1.53)	0.171(0.881)	0.098(0.415)	0.063(0.274)	0.042(0.212)	0.037(0.190)	0.036(0.175)	0.035(0.173)
12	50	1.22(6.53)	0.685(3.42)	0.382(1.97)	0.219(0.928)	0.141(0.613)	0.094(0.473)	0.083(0.424)	0.080(0.392)	0.078(0.386)
10	60	1.44(7.43)	0.725(3.56)	0.437(2.08)	0.226(1.37)	0.155(0.817)	0.108(0.585)	0.089(0.444)	0.082(0.417)	0.078(0.400)
2	300	3.33(22.6)	1.76(10.4)	1.03(6.24)	0.566(3.34)	0.325(2.13)	0.238(1.62)	0.202(1.28)	0.189(1.13)	0.186(1.06)
1	600	13.2(83.2)	7.68(41.6)	3.63(20.8)	1.79(10.4)	0.960(5.20)	0.566(3.34)	0.357(2.05)	0.287(1.77)	0.259(1.72)

Table 24. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
192	3.125	24.0(21.5)	23.8(21.5)	23.6(21.3)	23.4(21.4)	23.1(21.0)	22.7(20.3)	21.8(19.5)	20.9(18.6)	19.9(17.6)
30	10	23.1(20.7)	23.0(20.6)	22.8(20.4)	22.6(20.5)	22.2(20.1)	21.8(19.5)	21.0(18.7)	20.1(17.8)	19.1(16.8)
12	50	22.0(19.5)	21.8(19.5)	21.6(19.3)	21.4(19.4)	21.1(19.0)	20.7(18.3)	19.8(17.5)	18.9(16.6)	17.9(15.6)
10	60	21.7(19.4)	21.7(19.4)	21.4(19.2)	21.4(18.8)	20.9(18.5)	20.5(18.0)	19.7(17.4)	18.9(16.5)	17.9(15.6)
2	300	20.5(17.8)	20.4(17.9)	20.2(17.6)	20.1(17.5)	19.9(17.2)	19.3(16.6)	18.6(15.9)	17.7(15.1)	16.7(14.2)
1	600	18.5(15.9)	18.3(15.9)	18.4(15.9)	18.4(15.9)	18.3(15.9)	18.1(15.5)	17.7(15.2)	17.1(14.4)	16.2(13.5)

MID1 POWER MODE

SINC4 and Chop Disabled

Table 25. ADC Noise in μVRMS (μVPP) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	2.34	0.248(1.29)	0.138(0.682)	0.083(0.395)	0.047(0.238)	0.030(0.153)	0.021(0.097)	0.016(0.088)	0.014(0.087)	0.013(0.077)
1920	2.5	0.256(1.34)	0.142(0.705)	0.086(0.408)	0.049(0.246)	0.031(0.158)	0.022(0.100)	0.017(0.090)	0.015(0.090)	0.014(0.079)
960	5	0.363(1.89)	0.201(0.998)	0.121(0.578)	0.069(0.347)	0.044(0.223)	0.031(0.141)	0.024(0.128)	0.021(0.127)	0.019(0.112)
480	10	0.513(2.67)	0.285(1.41)	0.172(0.817)	0.097(0.491)	0.062(0.316)	0.044(0.200)	0.034(0.181)	0.029(0.179)	0.027(0.159)
240	20	0.725(3.78)	0.403(2.00)	0.243(1.16)	0.138(0.695)	0.087(0.446)	0.062(0.282)	0.048(0.256)	0.041(0.254)	0.039(0.225)
120	40	1.03(5.35)	0.570(2.82)	0.344(1.63)	0.195(0.982)	0.123(0.631)	0.088(0.399)	0.068(0.362)	0.059(0.359)	0.055(0.318)
96	50	1.15(5.98)	0.637(3.15)	0.384(1.83)	0.218(1.10)	0.138(0.706)	0.099(0.446)	0.076(0.405)	0.065(0.401)	0.061(0.355)
80	60	1.26(6.55)	0.698(3.46)	0.421(2.00)	0.238(1.20)	0.151(0.773)	0.108(0.489)	0.083(0.443)	0.072(0.439)	0.067(0.389)
60	80	1.45(7.56)	0.806(3.99)	0.486(2.31)	0.275(1.39)	0.174(0.893)	0.125(0.564)	0.096(0.512)	0.083(0.507)	0.077(0.450)
30	160	2.05(10.7)	1.14(5.64)	0.687(3.27)	0.389(1.96)	0.246(1.26)	0.177(0.798)	0.135(0.724)	0.117(0.717)	0.109(0.636)
15	320	2.62(15.1)	1.68(9.21)	0.931(5.72)	0.550(3.49)	0.330(1.99)	0.233(1.30)	0.187(1.08)	0.169(1.12)	0.153(0.860)
8	600	3.72(24.4)	2.40(14.4)	1.30(8.24)	0.720(4.46)	0.488(2.93)	0.317(1.87)	0.262(1.92)	0.233(1.45)	0.214(1.31)
4	1200	5.12(33.3)	3.32(22.3)	1.87(11.8)	1.07(7.02)	0.646(4.03)	0.477(3.08)	0.377(3.04)	0.334(2.33)	0.304(1.96)
2	2400	8.02(58.8)	4.71(30.0)	2.64(18.5)	1.55(10.3)	0.972(6.42)	0.676(4.42)	0.523(3.64)	0.465(3.11)	0.443(3.03)
1	4800	30.0(229)	15.6(156)	8.25(66.6)	4.22(33.3)	2.21(18.1)	1.29(9.62)	0.865(5.93)	0.688(4.74)	0.621(4.47)

Table 26. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	2.34	24.3(21.9)	24.1(21.8)	23.8(21.6)	23.7(21.3)	23.3(21.0)	22.8(20.6)	22.2(19.8)	21.4(18.8)	20.5(18.0)
1920	2.5	24.2(21.8)	24.1(21.8)	23.8(21.5)	23.6(21.3)	23.3(20.9)	22.8(20.6)	22.1(19.7)	21.3(18.7)	20.4(17.9)
960	5	23.7(21.3)	23.6(21.3)	23.3(21.0)	23.1(20.8)	22.8(20.4)	22.3(20.1)	21.6(19.2)	20.8(18.2)	19.9(17.4)
480	10	23.2(20.8)	23.1(20.8)	22.8(20.5)	22.6(20.3)	22.3(19.9)	21.8(19.6)	21.1(18.7)	20.3(17.7)	19.4(16.9)
240	20	22.7(20.3)	22.6(20.3)	22.3(20.0)	22.1(19.8)	21.8(19.4)	21.3(19.1)	20.6(18.2)	19.8(17.2)	18.9(16.4)
120	40	22.2(19.8)	22.1(19.8)	21.8(19.5)	21.6(19.3)	21.3(18.9)	20.8(18.6)	20.1(17.7)	19.3(16.7)	18.4(15.9)
96	50	22.1(19.7)	21.9(19.6)	21.6(19.4)	21.5(19.1)	21.1(18.8)	20.6(18.4)	20.0(17.6)	19.2(16.6)	18.3(15.7)
80	60	21.9(19.5)	21.8(19.5)	21.5(19.3)	21.3(19.0)	21.0(18.6)	20.5(18.3)	19.8(17.4)	19.1(16.4)	18.2(15.6)
60	80	21.7(19.3)	21.6(19.3)	21.3(19.0)	21.1(18.8)	20.8(18.4)	20.3(18.1)	19.6(17.2)	18.8(16.2)	17.9(15.4)
30	160	21.2(18.8)	21.1(18.8)	20.8(18.5)	20.6(18.3)	20.3(17.9)	19.8(17.6)	19.1(16.7)	18.3(15.7)	17.4(14.9)
15	320	20.9(18.3)	20.5(18.1)	20.4(17.7)	20.1(17.5)	19.9(17.3)	19.4(16.9)	18.7(16.1)	17.8(15.1)	17.0(14.5)
8	600	20.4(17.6)	20.0(17.4)	19.9(17.2)	19.7(17.1)	19.3(16.7)	18.9(16.3)	18.2(15.3)	17.4(14.7)	16.5(13.9)
4	1200	19.9(17.2)	19.5(16.8)	19.4(16.7)	19.2(16.4)	18.9(16.2)	18.3(15.6)	17.7(14.7)	16.8(14.0)	16.0(13.3)
2	2400	19.2(16.4)	19.0(16.3)	18.9(16.0)	18.6(15.9)	18.3(15.6)	17.8(15.1)	17.2(14.4)	16.4(13.6)	15.4(12.7)
1	4800	17.3(14.4)	17.3(14.0)	17.2(14.2)	17.2(14.2)	17.1(14.1)	16.9(14.0)	16.5(13.7)	15.8(13.0)	14.9(12.1)

Table 27. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 5 V, V_{REF} = 5 V, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	2.34	25.4(22.8)	24.9(22.5)	24.8(22.5)	24.6(22.1)	24.3(21.9)	23.9(21.4)	23.3(20.8)	22.4(19.9)	21.5(19.0)
1920	2.5	25.3(22.8)	24.9(22.5)	24.7(22.4)	24.6(22.1)	24.3(21.9)	23.8(21.3)	23.2(20.7)	22.3(19.9)	21.4(19.0)
960	5	24.8(22.3)	24.4(22.0)	24.2(21.9)	24.1(21.6)	23.8(21.4)	23.3(20.8)	22.7(20.2)	21.8(19.4)	20.9(18.5)
480	10	24.3(21.8)	23.9(21.5)	23.7(21.4)	23.6(21.1)	23.3(20.9)	22.8(20.3)	22.2(19.7)	21.3(18.9)	20.4(18.0)
240	20	23.8(21.3)	23.4(21.0)	23.2(20.9)	23.1(20.6)	22.8(20.4)	22.3(19.8)	21.7(19.2)	20.8(18.4)	19.9(17.5)
120	40	23.3(20.8)	22.9(20.5)	22.7(20.4)	22.6(20.1)	22.3(19.9)	21.8(19.3)	21.2(18.7)	20.3(17.9)	19.4(17.0)
96	50	23.1(20.6)	22.7(20.3)	22.6(20.3)	22.4(19.9)	22.1(19.7)	21.6(19.2)	21.1(18.6)	20.1(17.7)	19.2(16.8)
80	60	23.0(20.5)	22.6(20.2)	22.5(20.1)	22.3(19.8)	22.0(19.6)	21.5(19.0)	20.9(18.4)	20.0(17.6)	19.1(16.7)
60	80	22.8(20.3)	22.4(20.0)	22.2(19.9)	22.1(19.6)	21.8(19.4)	21.3(18.8)	20.7(18.2)	19.8(17.4)	18.9(16.5)
30	160	22.3(19.8)	21.9(19.5)	21.7(19.4)	21.6(19.1)	21.3(18.9)	20.8(18.3)	20.2(17.7)	19.3(16.9)	18.4(16.0)
15	320	21.8(19.1)	21.5(18.9)	21.3(18.6)	21.1(18.5)	20.9(18.4)	20.4(17.7)	19.7(16.9)	18.9(16.5)	18.0(15.6)
8	600	21.3(18.6)	20.9(18.4)	20.8(18.3)	20.7(18.1)	20.3(17.7)	19.9(17.3)	19.3(16.6)	18.4(15.8)	17.5(14.8)
4	1200	20.8(18.1)	20.5(17.8)	20.3(17.6)	20.1(17.2)	19.9(17.0)	19.4(16.8)	18.7(15.9)	17.9(15.4)	16.9(14.4)
2	2400	20.1(17.3)	19.8(17.1)	19.7(16.9)	19.6(16.9)	19.3(16.5)	18.8(16.0)	18.2(15.4)	17.4(14.7)	16.5(13.8)
1	4800	17.4(14.4)	17.4(14.5)	17.4(14.5)	17.4(14.4)	17.3(14.5)	17.2(14.3)	17.1(14.2)	16.6(13.8)	15.9(13.0)

SINC3 and Chop Disabled

Table 28. ADC Noise in µVRMS (µVPP) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	2.34	0.278(1.46)	0.148(0.790)	0.091(0.471)	0.051(0.277)	0.034(0.180)	0.020(0.111)	0.017(0.099)	0.016(0.089)	0.015(0.079)
1920	2.5	0.288(1.51)	0.153(0.817)	0.094(0.487)	0.053(0.286)	0.035(0.186)	0.021(0.115)	0.018(0.102)	0.016(0.092)	0.015(0.082)
960	5	0.407(2.14)	0.216(1.16)	0.133(0.688)	0.075(0.405)	0.049(0.263)	0.030(0.162)	0.025(0.144)	0.023(0.131)	0.021(0.116)
480	10	0.576(3.02)	0.306(1.63)	0.188(0.973)	0.106(0.573)	0.070(0.372)	0.042(0.230)	0.036(0.204)	0.032(0.185)	0.030(0.164)
240	20	0.814(4.27)	0.433(2.31)	0.266(1.38)	0.150(0.810)	0.098(0.526)	0.059(0.325)	0.051(0.289)	0.046(0.261)	0.043(0.232)
120	40	1.15(6.04)	0.612(3.27)	0.376(1.95)	0.213(1.15)	0.139(0.743)	0.084(0.459)	0.072(0.408)	0.065(0.369)	0.061(0.328)
96	50	1.29(6.76)	0.685(3.65)	0.421(2.18)	0.238(1.28)	0.156(0.831)	0.094(0.514)	0.081(0.457)	0.073(0.413)	0.068(0.367)
80	60	1.41(7.40)	0.750(4.00)	0.461(2.38)	0.260(1.40)	0.170(0.910)	0.103(0.563)	0.088(0.500)	0.080(0.452)	0.074(0.402)
60	80	1.63(8.55)	0.866(4.62)	0.532(2.75)	0.301(1.62)	0.197(1.05)	0.119(0.650)	0.102(0.578)	0.092(0.522)	0.086(0.464)
30	160	2.30(12.1)	1.22(6.53)	0.753(3.89)	0.425(2.29)	0.278(1.49)	0.168(0.919)	0.144(0.817)	0.130(0.738)	0.121(0.657)
15	320	2.81(17.5)	1.83(10.2)	1.03(6.76)	0.622(3.34)	0.393(2.43)	0.254(1.51)	0.211(1.18)	0.176(1.09)	0.164(0.893)
8	600	4.10(27.6)	2.46(13.5)	1.40(8.02)	0.778(5.68)	0.510(3.10)	0.346(2.12)	0.290(1.75)	0.243(1.55)	0.237(1.55)
4	1200	7.14(44.3)	4.14(26.1)	2.25(15.3)	1.26(8.17)	0.804(5.25)	0.543(3.17)	0.400(2.75)	0.348(2.36)	0.344(2.20)
2	2400	35.7(187)	17.4(107)	8.92(49.8)	4.59(27.5)	2.37(16.2)	1.27(7.98)	0.776(5.44)	0.572(3.93)	0.480(3.69)
1	4800	275(1540)	138(748)	70.0(374)	35.1(190)	17.4(93.5)	8.77(46.1)	4.34(24.9)	2.31(13.2)	1.26(8.01)

Table 29. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	2.34	24.1(21.7)	24.0(21.6)	23.7(21.3)	23.5(21.1)	23.1(20.7)	22.9(20.4)	22.1(19.6)	21.2(18.7)	20.3(17.9)
1920	2.5	24.1(21.7)	24.0(21.5)	23.7(21.3)	23.5(21.1)	23.1(20.7)	22.8(20.4)	22.0(19.5)	21.2(18.7)	20.3(17.9)
960	5	23.6(21.2)	23.5(21.0)	23.2(20.8)	23.0(20.6)	22.6(20.2)	22.3(19.9)	21.5(19.0)	20.7(18.2)	19.8(17.4)
480	10	23.1(20.7)	23.0(20.5)	22.7(20.3)	22.5(20.1)	22.1(19.7)	21.8(19.4)	21.0(18.5)	20.2(17.7)	19.3(16.9)
240	20	22.6(20.2)	22.5(20.0)	22.2(19.8)	22.0(19.6)	21.6(19.2)	21.3(18.9)	20.5(18.0)	19.7(17.2)	18.8(16.4)
120	40	22.1(19.7)	22.0(19.5)	21.7(19.3)	21.5(19.1)	21.1(18.7)	20.8(18.4)	20.0(17.5)	19.2(16.7)	18.3(15.9)
96	50	21.9(19.5)	21.8(19.4)	21.5(19.1)	21.3(18.9)	20.9(18.5)	20.7(18.2)	19.9(17.4)	19.0(16.5)	18.1(15.7)
80	60	21.8(19.4)	21.7(19.3)	21.4(19.0)	21.2(18.8)	20.8(18.4)	20.5(18.1)	19.8(17.3)	18.9(16.4)	18.0(15.6)
60	80	21.6(19.2)	21.5(19.0)	21.2(18.8)	21.0(18.6)	20.6(18.2)	20.3(17.9)	19.5(17.0)	18.7(16.2)	17.8(15.4)
30	160	21.1(18.7)	21.0(18.5)	20.7(18.3)	20.5(18.1)	20.1(17.7)	19.8(17.4)	19.0(16.5)	18.2(15.7)	17.3(14.9)
15	320	20.8(18.1)	20.4(17.9)	20.2(17.5)	19.9(17.5)	19.6(17.0)	19.2(16.7)	18.5(16.0)	17.8(15.1)	16.9(14.4)
8	600	20.2(17.5)	20.0(17.5)	19.8(17.2)	19.6(16.7)	19.2(16.6)	18.8(16.2)	18.0(15.4)	17.3(14.6)	16.3(13.6)
4	1200	19.4(16.8)	19.2(16.5)	19.1(16.3)	18.9(16.2)	18.6(15.9)	18.1(15.6)	17.6(14.8)	16.8(14.0)	15.8(13.1)
2	2400	17.1(14.7)	17.1(14.5)	17.1(14.6)	17.1(14.5)	17.0(14.2)	16.9(14.3)	16.6(13.8)	16.1(13.3)	15.3(12.4)
1	4800	14.1(11.7)	14.1(11.7)	14.1(11.7)	14.1(11.7)	14.1(11.7)	14.1(11.7)	14.1(11.6)	14.0(11.5)	13.9(11.3)

Table 30. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 5 V, V_{REF} = 5 V, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	2.34	25.1(22.7)	24.8(22.3)	24.7(22.2)	24.4(21.8)	24.2(21.8)	23.7(21.3)	23.2(20.6)	22.2(19.8)	21.3(18.9)
1920	2.5	25.1(22.7)	24.8(22.3)	24.6(22.1)	24.3(21.8)	24.1(21.7)	23.7(21.2)	23.1(20.6)	22.2(19.8)	21.3(18.8)
960	5	24.6(22.2)	24.3(21.8)	24.1(21.6)	23.8(21.3)	23.6(21.2)	23.2(20.7)	22.6(20.1)	21.7(19.3)	20.8(18.3)
480	10	24.1(21.7)	23.8(21.3)	23.6(21.1)	23.3(20.8)	23.1(20.7)	22.7(20.2)	22.1(19.6)	21.2(18.8)	20.3(17.8)
240	20	23.6(21.2)	23.3(20.8)	23.1(20.6)	22.8(20.3)	22.6(20.2)	22.2(19.7)	21.6(19.1)	20.7(18.3)	19.8(17.3)
120	40	23.1(20.7)	22.8(20.3)	22.6(20.1)	22.3(19.8)	22.1(19.7)	21.7(19.2)	21.1(18.6)	20.2(17.8)	19.3(16.8)
96	50	22.9(20.5)	22.6(20.1)	22.5(20.0)	22.2(19.6)	22.0(19.6)	21.5(19.1)	20.9(18.4)	20.0(17.6)	19.1(16.7)
80	60	22.8(20.4)	22.5(20.0)	22.3(19.8)	22.1(19.5)	21.8(19.5)	21.4(19.0)	20.8(18.3)	19.9(17.5)	19.0(16.5)
60	80	22.6(20.2)	22.3(19.8)	22.1(19.6)	21.8(19.3)	21.6(19.2)	21.2(18.7)	20.6(18.1)	19.7(17.3)	18.8(16.3)
30	160	22.1(19.7)	21.8(19.3)	21.6(19.1)	21.3(18.8)	21.1(18.7)	20.7(18.2)	20.1(17.6)	19.2(16.8)	18.3(15.8)
15	320	21.6(19.1)	21.4(19.1)	21.1(18.5)	21.0(18.4)	20.7(18.1)	20.1(17.5)	19.7(17.1)	18.7(16.4)	17.7(15.4)
8	600	21.2(18.5)	20.9(18.1)	20.7(18.1)	20.6(18.0)	20.2(17.6)	19.7(17.1)	19.1(16.5)	18.3(15.8)	17.5(14.7)
4	1200	19.9(17.3)	19.7(17.1)	19.7(17.1)	19.7(16.9)	19.4(16.8)	19.1(16.5)	18.6(15.8)	17.8(15.0)	16.8(14.2)
2	2400	17.1(14.7)	17.1(14.7)	17.2(14.7)	17.1(14.7)	17.1(14.6)	17.0(14.6)	17.0(14.3)	16.7(14.2)	16.2(13.4)
1	4800	14.2(11.6)	14.1(11.6)	14.1(11.6)	14.2(11.6)	14.1(11.7)	14.1(11.7)	14.1(11.6)	14.1(11.5)	14.1(11.5)

Post Filters, SINC3 and Chop Disabled

Table 31. ADC Noise in µVRMS (µVPP) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Data Rate (SPS)	PGA GAIN								
	1	2	4	8	16	32	64	128	256
16.67	1.08(4.75)	0.721(3.26)	0.374(1.59)	0.215(0.928)	0.133(0.615)	0.094(0.418)	0.076(0.343)	0.065(0.297)	0.060(0.237)
20	1.20(5.05)	0.731(3.56)	0.424(1.78)	0.234(1.04)	0.145(0.651)	0.102(0.436)	0.080(0.369)	0.066(0.324)	0.065(0.276)
25	1.27(5.64)	0.831(4.01)	0.466(1.93)	0.243(1.08)	0.159(0.758)	0.111(0.468)	0.089(0.422)	0.073(0.358)	0.070(0.309)
27.27	1.32(5.95)	0.849(4.16)	0.485(2.15)	0.251(1.23)	0.172(0.798)	0.125(0.518)	0.107(0.464)	0.082(0.371)	0.077(0.327)

Table 32. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Data Rate (SPS)	PGA GAIN								
	1	2	4	8	16	32	64	128	256
16.67	22.1(20.0)	21.7(19.5)	21.7(19.6)	21.5(19.4)	21.2(19.0)	20.7(18.5)	20.0(17.8)	19.2(17.0)	18.3(16.3)
20	22.0(19.9)	21.7(19.4)	21.5(19.4)	21.4(19.2)	21.0(18.9)	20.5(18.5)	19.9(17.7)	19.2(16.9)	18.2(16.1)
25	21.9(19.8)	21.5(19.2)	21.4(19.3)	21.3(19.1)	20.9(18.7)	20.4(18.3)	19.7(17.5)	19.0(16.7)	18.1(15.9)
27.27	21.8(19.7)	21.5(19.2)	21.3(19.1)	21.2(19.0)	20.8(18.6)	20.3(18.2)	19.5(17.4)	18.9(16.7)	17.9(15.9)

Fast Settling, Average=16, SINC4 and Chop Disabled

Table 33. ADC Noise in µVRMS (µVPP) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
96	3.125	0.372(1.86)	0.240(1.29)	0.136(0.637)	0.081(0.402)	0.049(0.241)	0.036(0.170)	0.027(0.129)	0.024(0.107)	0.022(0.102)
30	10	0.666(3.32)	0.429(2.30)	0.243(1.14)	0.144(0.719)	0.088(0.432)	0.065(0.304)	0.048(0.230)	0.042(0.192)	0.039(0.182)
6	50	1.49(7.43)	0.959(5.15)	0.542(2.55)	0.322(1.61)	0.196(0.965)	0.145(0.680)	0.108(0.515)	0.095(0.429)	0.088(0.406)
5	60	1.64(8.13)	1.03(5.35)	0.568(3.14)	0.345(1.81)	0.224(1.04)	0.153(0.722)	0.126(0.613)	0.101(0.479)	0.098(0.434)
2	150	2.85(16.3)	1.57(8.61)	1.00(5.64)	0.514(3.08)	0.390(2.47)	0.241(1.41)	0.174(0.863)	0.167(0.852)	0.154(0.828)
1	300	4.01(22.6)	2.55(13.8)	1.31(7.13)	0.762(4.27)	0.495(2.99)	0.318(2.00)	0.256(1.51)	0.242(1.44)	0.227(1.34)

Table 34. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
96	3.125	23.7(21.4)	23.3(20.9)	23.1(20.9)	22.9(20.6)	22.6(20.3)	22.0(19.8)	21.5(19.2)	20.6(18.5)	19.8(17.6)
30	10	22.8(20.5)	22.5(20.1)	22.3(20.1)	22.0(19.7)	21.8(19.5)	21.2(19.0)	20.6(18.4)	19.8(17.6)	18.9(16.7)
6	50	21.7(19.4)	21.3(18.9)	21.1(18.9)	20.9(18.6)	20.6(18.3)	20.0(17.8)	19.5(17.2)	18.6(16.5)	17.8(15.6)
5	60	21.5(19.2)	21.2(18.8)	21.1(18.6)	20.8(18.4)	20.4(18.2)	20.0(17.7)	19.2(17.0)	18.6(16.3)	17.6(15.5)
2	150	20.7(18.2)	20.6(18.1)	20.2(17.8)	20.2(17.6)	19.6(16.9)	19.3(16.8)	18.8(16.5)	17.8(15.5)	17.0(14.5)
1	300	20.3(17.8)	19.9(17.5)	19.9(17.4)	19.6(17.2)	19.3(16.7)	18.9(16.3)	18.2(15.7)	17.3(14.7)	16.4(13.8)

Fast Settling, Average=16, SINC3 and Chop Disabled

Table 35. ADC Noise in µVRMS (µVPP) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
96	3.125	0.379(2.00)	0.244(1.29)	0.141(0.723)	0.082(0.411)	0.051(0.247)	0.037(0.177)	0.027(0.131)	0.025(0.112)	0.023(0.103)
30	10	0.679(3.59)	0.437(2.31)	0.251(1.29)	0.147(0.736)	0.092(0.443)	0.065(0.317)	0.048(0.234)	0.044(0.200)	0.041(0.185)
6	50	1.52(8.02)	0.976(5.16)	0.562(2.89)	0.329(1.64)	0.206(0.990)	0.146(0.708)	0.107(0.524)	0.099(0.448)	0.091(0.413)
5	60	1.78(8.61)	1.10(5.60)	0.576(3.41)	0.352(1.81)	0.228(1.12)	0.155(0.728)	0.123(0.613)	0.114(0.487)	0.099(0.448)
2	150	3.58(19.6)	1.83(10.4)	1.09(6.24)	0.589(2.97)	0.354(1.78)	0.245(1.34)	0.193(0.975)	0.171(0.884)	0.160(0.850)
1	300	13.7(71.3)	6.91(35.6)	3.85(23.8)	1.93(10.4)	0.977(5.20)	0.550(3.34)	0.362(2.05)	0.252(1.49)	0.223(1.36)

Table 36. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
96	3.125	23.7(21.3)	23.3(20.9)	23.1(20.7)	22.9(20.5)	22.5(20.3)	22.0(19.8)	21.5(19.2)	20.6(18.4)	19.7(17.5)
30	10	22.8(20.4)	22.4(20.0)	22.2(19.9)	22.0(19.7)	21.7(19.4)	21.2(18.9)	20.6(18.3)	19.8(17.6)	18.9(16.7)
6	50	21.7(19.3)	21.3(18.9)	21.1(18.7)	20.9(18.5)	20.5(18.3)	20.0(17.8)	19.5(17.2)	18.6(16.4)	17.7(15.5)
5	60	21.4(19.1)	21.1(18.8)	21.0(18.5)	20.8(18.4)	20.4(18.1)	19.9(17.7)	19.3(17.0)	18.4(16.3)	17.6(15.4)
2	150	20.4(18.0)	20.4(17.9)	20.1(17.6)	20.0(17.7)	19.8(17.4)	19.3(16.8)	18.6(16.3)	17.8(15.4)	16.9(14.5)
1	300	18.5(16.1)	18.5(16.1)	18.3(15.7)	18.3(15.9)	18.3(15.9)	18.1(15.5)	17.7(15.2)	17.2(14.7)	16.4(13.8)

LOW POWER MODE

SINC4 and Chop Disabled

Table 37. ADC Noise in µVRMS (µVPP) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	1.17	0.264(1.29)	0.155(0.808)	0.094(0.458)	0.048(0.233)	0.030(0.144)	0.024(0.119)	0.017(0.081)	0.013(0.063)	0.012(0.060)
1920	1.25	0.273(1.33)	0.160(0.835)	0.097(0.473)	0.049(0.241)	0.031(0.149)	0.025(0.123)	0.017(0.084)	0.014(0.066)	0.013(0.062)
960	2.5	0.387(1.89)	0.226(1.18)	0.138(0.669)	0.070(0.341)	0.044(0.211)	0.035(0.174)	0.024(0.119)	0.019(0.093)	0.018(0.088)
480	5	0.547(2.67)	0.320(1.67)	0.195(0.947)	0.099(0.483)	0.062(0.298)	0.050(0.246)	0.034(0.168)	0.027(0.131)	0.025(0.124)
240	10	0.773(3.78)	0.453(2.36)	0.275(1.34)	0.140(0.683)	0.088(0.421)	0.071(0.348)	0.049(0.238)	0.039(0.185)	0.036(0.175)
120	20	1.09(5.34)	0.640(3.34)	0.389(1.89)	0.198(0.965)	0.124(0.595)	0.100(0.492)	0.069(0.336)	0.055(0.262)	0.051(0.248)
60	40	1.55(7.55)	0.906(4.73)	0.550(2.68)	0.280(1.37)	0.176(0.842)	0.141(0.696)	0.097(0.476)	0.077(0.371)	0.072(0.351)
48	50	1.73(8.44)	1.01(5.28)	0.615(2.99)	0.313(1.53)	0.196(0.941)	0.158(0.778)	0.109(0.532)	0.087(0.415)	0.080(0.392)
40	60	1.89(9.25)	1.11(5.79)	0.674(3.28)	0.343(1.67)	0.215(1.03)	0.173(0.853)	0.119(0.583)	0.095(0.454)	0.088(0.429)
30	80	2.19(10.7)	1.28(6.68)	0.778(3.79)	0.395(1.93)	0.248(1.19)	0.199(0.984)	0.137(0.673)	0.109(0.524)	0.101(0.496)
15	160	2.71(13.4)	1.91(9.05)	1.07(5.79)	0.548(2.60)	0.366(2.23)	0.246(1.49)	0.176(1.00)	0.149(0.854)	0.141(0.818)
8	300	3.86(21.1)	2.23(12.8)	1.38(7.87)	0.780(4.46)	0.531(2.71)	0.370(2.06)	0.254(1.32)	0.230(1.39)	0.213(1.19)
4	600	5.52(31.5)	3.22(20.5)	1.87(10.2)	1.11(6.68)	0.741(4.57)	0.509(3.41)	0.361(2.19)	0.325(2.16)	0.286(1.75)
2	1200	8.00(49.3)	4.90(31.5)	2.90(19.8)	1.58(10.4)	0.970(5.81)	0.707(3.81)	0.520(3.08)	0.427(2.68)	0.422(2.80)
1	2400	29.5(204)	15.6(119)	8.04(61.5)	4.33(54.6)	2.32(20.0)	1.31(9.51)	0.850(6.44)	0.635(4.87)	0.591(4.25)

Table 38. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	1.17	24.2(21.9)	23.9(21.6)	23.7(21.4)	23.6(21.4)	23.3(21.0)	22.6(20.3)	22.2(19.9)	21.5(19.2)	20.6(18.3)
1920	1.25	24.1(21.8)	23.9(21.5)	23.6(21.3)	23.6(21.3)	23.3(21.0)	22.6(20.3)	22.1(19.8)	21.4(19.2)	20.6(18.3)
960	2.5	23.6(21.3)	23.4(21.0)	23.1(20.8)	23.1(20.8)	22.8(20.5)	22.1(19.8)	21.6(19.3)	20.9(18.7)	20.1(17.8)
480	5	23.1(20.8)	22.9(20.5)	22.6(20.3)	22.6(20.3)	22.3(20.0)	21.6(19.3)	21.1(18.8)	20.4(18.2)	19.6(17.3)
240	10	22.6(20.3)	22.4(20.0)	22.1(19.8)	22.1(19.8)	21.8(19.5)	21.1(18.8)	20.6(18.3)	19.9(17.7)	19.1(16.8)
120	20	22.1(19.8)	21.9(19.5)	21.6(19.3)	21.6(19.3)	21.3(19.0)	20.6(18.3)	20.1(17.8)	19.4(17.2)	18.6(16.3)
60	40	21.6(19.3)	21.4(19.0)	21.1(18.8)	21.1(18.8)	20.8(18.5)	20.1(17.8)	19.6(17.3)	18.9(16.7)	18.1(15.8)
48	50	21.5(19.2)	21.2(18.9)	21.0(18.7)	20.9(18.6)	20.6(18.3)	19.9(17.6)	19.5(17.2)	18.8(16.5)	17.9(15.6)
40	60	21.3(19.0)	21.1(18.7)	20.8(18.5)	20.8(18.5)	20.5(18.2)	19.8(17.5)	19.3(17.0)	18.7(16.4)	17.8(15.5)
30	80	21.1(18.8)	20.9(18.5)	20.6(18.3)	20.6(18.3)	20.3(18.0)	19.6(17.3)	19.1(16.8)	18.4(16.2)	17.6(15.3)
15	160	20.8(18.5)	20.3(18.1)	20.2(17.7)	20.1(17.9)	19.7(17.1)	19.3(16.7)	18.8(16.3)	18.0(15.5)	17.1(14.5)
8	300	20.3(17.9)	20.1(17.6)	19.8(17.3)	19.6(17.1)	19.2(16.8)	18.7(16.2)	18.2(15.9)	17.4(14.8)	16.5(14.0)
4	600	19.8(17.3)	19.6(16.9)	19.3(16.9)	19.1(16.5)	18.7(16.1)	18.2(15.5)	17.7(15.1)	16.9(14.1)	16.1(13.4)
2	1200	19.3(16.6)	19.0(16.3)	18.7(15.9)	18.6(15.9)	18.3(15.7)	17.8(15.3)	17.2(14.6)	16.5(13.8)	15.5(12.8)
1	2400	17.4(14.6)	17.3(14.4)	17.2(14.3)	17.1(13.5)	17.0(13.9)	16.9(14.0)	16.5(13.6)	15.9(13.0)	15.0(12.2)

Table 39. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 5 V, V_{REF} = 5 V, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	1.17	25.1(22.9)	24.9(22.6)	24.7(22.4)	24.6(22.1)	24.3(22.0)	23.9(21.4)	23.3(21.1)	22.7(20.3)	21.7(19.3)
1920	1.25	25.1(22.8)	24.8(22.5)	24.7(22.3)	24.5(22.1)	24.3(21.9)	23.9(21.4)	23.3(21.1)	22.6(20.2)	21.7(19.3)
960	2.5	24.6(22.3)	24.3(22.0)	24.2(21.8)	24.0(21.6)	23.8(21.4)	23.4(20.9)	22.8(20.6)	22.1(19.7)	21.2(18.8)
480	5	24.1(21.8)	23.8(21.5)	23.7(21.3)	23.5(21.1)	23.3(20.9)	22.9(20.4)	22.3(20.1)	21.6(19.2)	20.7(18.3)
240	10	23.6(21.3)	23.3(21.0)	23.2(20.8)	23.0(20.6)	22.8(20.4)	22.4(19.9)	21.8(19.6)	21.1(18.7)	20.2(17.8)
120	20	23.1(20.8)	22.8(20.5)	22.7(20.3)	22.5(20.1)	22.3(19.9)	21.9(19.4)	21.3(19.1)	20.6(18.2)	19.7(17.3)
60	40	22.6(20.3)	22.3(20.0)	22.2(19.8)	22.0(19.6)	21.8(19.4)	21.4(18.9)	20.8(18.6)	20.1(17.7)	19.2(16.8)
48	50	22.4(20.2)	22.2(19.9)	22.0(19.6)	21.9(19.4)	21.6(19.3)	21.2(18.7)	20.6(18.4)	20.0(17.5)	19.0(16.6)
40	60	22.3(20.0)	22.0(19.7)	21.9(19.5)	21.7(19.3)	21.5(19.1)	21.1(18.6)	20.5(18.3)	19.8(17.4)	18.9(16.5)
30	80	22.1(19.8)	21.8(19.5)	21.7(19.3)	21.5(19.1)	21.3(18.9)	20.9(18.4)	20.3(18.1)	19.6(17.2)	18.7(16.3)
15	160	21.8(19.5)	21.5(18.9)	21.3(18.8)	21.0(18.7)	20.7(18.4)	20.4(17.9)	19.5(17.1)	18.9(16.5)	18.1(15.8)
8	300	21.3(18.8)	21.0(18.4)	20.9(18.4)	20.6(18.1)	20.4(17.7)	19.9(17.4)	19.2(16.9)	18.4(15.9)	17.6(15.1)
4	600	20.8(18.0)	20.5(18.1)	20.4(17.7)	20.1(17.6)	19.8(17.3)	19.4(16.9)	18.8(16.2)	17.9(15.4)	17.1(14.7)
2	1200	20.1(17.3)	19.8(17.0)	19.7(16.9)	19.6(16.8)	19.2(16.3)	18.8(16.2)	18.2(15.4)	17.5(15.0)	16.6(13.9)
1	2400	17.4(14.6)	17.4(14.4)	17.4(14.5)	17.4(14.3)	17.4(14.4)	17.2(14.3)	17.0(13.9)	16.7(13.9)	16.0(13.1)

SINC3 and Chop Disabled

Table 40. ADC Noise in μVRMS (μVPP) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	1.17	0.284(1.40)	0.172(0.898)	0.100(0.521)	0.054(0.287)	0.035(0.159)	0.026(0.131)	0.018(0.084)	0.015(0.072)	0.013(0.067)
1920	1.25	0.294(1.45)	0.178(0.928)	0.103(0.538)	0.056(0.297)	0.036(0.165)	0.027(0.135)	0.018(0.087)	0.015(0.075)	0.014(0.069)
960	2.5	0.416(2.05)	0.251(1.31)	0.146(0.761)	0.079(0.420)	0.051(0.233)	0.038(0.191)	0.026(0.123)	0.021(0.106)	0.019(0.097)
480	5	0.588(2.90)	0.355(1.86)	0.206(1.08)	0.112(0.594)	0.073(0.330)	0.054(0.270)	0.036(0.174)	0.030(0.150)	0.027(0.138)
240	10	0.831(4.10)	0.502(2.63)	0.292(1.52)	0.159(0.840)	0.103(0.466)	0.076(0.382)	0.051(0.245)	0.043(0.212)	0.038(0.195)
120	20	1.18(5.79)	0.710(3.71)	0.412(2.15)	0.224(1.19)	0.145(0.659)	0.107(0.541)	0.073(0.347)	0.060(0.300)	0.054(0.275)
60	40	1.66(8.19)	1.00(5.25)	0.583(3.05)	0.317(1.68)	0.205(0.933)	0.152(0.765)	0.103(0.491)	0.085(0.424)	0.076(0.390)
48	50	1.86(9.16)	1.12(5.87)	0.652(3.40)	0.354(1.88)	0.229(1.04)	0.170(0.855)	0.115(0.549)	0.096(0.474)	0.085(0.436)
40	60	2.04(10.0)	1.23(6.43)	0.714(3.73)	0.388(2.06)	0.251(1.14)	0.186(0.936)	0.126(0.601)	0.105(0.519)	0.094(0.477)
30	80	2.35(11.6)	1.42(7.42)	0.825(4.31)	0.448(2.38)	0.290(1.32)	0.215(1.08)	0.145(0.694)	0.121(0.599)	0.108(0.551)
15	160	3.17(15.4)	1.96(9.36)	1.13(6.68)	0.619(3.79)	0.395(2.48)	0.296(1.69)	0.220(1.13)	0.174(0.900)	0.157(0.912)
8	300	4.02(26.7)	2.69(15.7)	1.41(7.50)	0.810(3.97)	0.512(2.93)	0.367(2.11)	0.266(1.61)	0.243(1.42)	0.221(1.36)
4	600	6.97(49.0)	4.16(26.6)	2.31(14.3)	1.32(7.50)	0.792(4.86)	0.540(3.55)	0.403(2.94)	0.333(2.10)	0.317(1.98)
2	1200	34.3(175)	18.2(95.0)	9.53(53.5)	4.55(24.1)	2.38(13.7)	1.32(8.07)	0.811(5.11)	0.532(3.42)	0.449(2.62)
1	2400	265(1570)	138(748)	65.7(356)	34.8(190)	17.5(93.5)	8.86(46.8)	4.30(23.4)	2.29(12.5)	0.808(2.05)

Table 41. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	1.17	24.1(21.8)	23.8(21.4)	23.6(21.2)	23.5(21.1)	23.1(20.9)	22.5(20.2)	22.1(19.8)	21.3(19.0)	20.5(18.2)
1920	1.25	24.0(21.7)	23.7(21.4)	23.5(21.1)	23.4(21.0)	23.0(20.9)	22.5(20.1)	22.0(19.8)	21.3(19.0)	20.5(18.1)
960	2.5	23.5(21.2)	23.2(20.9)	23.0(20.6)	22.9(20.5)	22.5(20.4)	22.0(19.6)	21.5(19.3)	20.8(18.5)	20.0(17.6)
480	5	23.0(20.7)	22.7(20.4)	22.5(20.1)	22.4(20.0)	22.0(19.9)	21.5(19.1)	21.0(18.8)	20.3(18.0)	19.5(17.1)
240	10	22.5(20.2)	22.2(19.9)	22.0(19.6)	21.9(19.5)	21.5(19.4)	21.0(18.6)	20.5(18.3)	19.8(17.5)	19.0(16.6)
120	20	22.0(19.7)	21.7(19.4)	21.5(19.1)	21.4(19.0)	21.0(18.9)	20.5(18.1)	20.0(17.8)	19.3(17.0)	18.5(16.1)
60	40	21.5(19.2)	21.2(18.9)	21.0(18.6)	20.9(18.5)	20.5(18.4)	20.0(17.6)	19.5(17.3)	18.8(16.5)	18.0(15.6)
48	50	21.4(19.1)	21.1(18.7)	20.9(18.5)	20.7(18.3)	20.4(18.2)	19.8(17.5)	19.4(17.1)	18.6(16.3)	17.8(15.5)
40	60	21.2(18.9)	21.0(18.6)	20.7(18.4)	20.6(18.2)	20.2(18.1)	19.7(17.3)	19.2(17.0)	18.5(16.2)	17.7(15.3)
30	80	21.0(18.7)	20.7(18.4)	20.5(18.1)	20.4(18.0)	20.0(17.9)	19.5(17.1)	19.0(16.8)	18.3(16.0)	17.5(15.1)
15	160	20.6(18.3)	20.3(18.0)	20.1(17.5)	19.9(17.3)	19.6(16.9)	19.0(16.5)	18.4(16.1)	17.8(15.4)	16.9(14.4)
8	300	20.2(17.5)	19.8(17.3)	19.8(17.3)	19.6(17.3)	19.2(16.7)	18.7(16.2)	18.2(15.6)	17.3(14.8)	16.4(13.8)
4	600	19.5(16.6)	19.2(16.5)	19.0(16.4)	18.9(16.3)	18.6(16.0)	18.1(15.4)	17.6(14.7)	16.8(14.2)	15.9(13.3)
2	1200	17.2(14.8)	17.1(14.7)	17.0(14.5)	17.1(14.7)	17.0(14.5)	16.9(14.2)	16.6(13.9)	16.2(13.5)	15.4(12.9)
1	2400	14.2(11.6)	14.1(11.7)	14.2(11.8)	14.1(11.7)	14.1(11.7)	14.1(11.7)	14.1(11.7)	14.1(11.6)	14.6(13.2)

Table 42. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 5 V, V_{REF} = 5 V, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
2047	1.17	25.0(22.6)	24.7(22.5)	24.6(22.2)	24.5(22.0)	24.1(21.7)	23.7(21.2)	23.1(20.9)	22.5(20.1)	21.5(19.2)
1920	1.25	25.0(22.5)	24.7(22.4)	24.6(22.2)	24.4(21.9)	24.0(21.7)	23.6(21.2)	23.0(20.9)	22.4(20.1)	21.5(19.1)
960	2.5	24.5(22.0)	24.2(21.9)	24.1(21.7)	23.9(21.4)	23.5(21.2)	23.1(20.7)	22.5(20.4)	21.9(19.6)	21.0(18.6)
480	5	24.0(21.5)	23.7(21.4)	23.6(21.2)	23.4(20.9)	23.0(20.7)	22.6(20.2)	22.0(19.9)	21.4(19.1)	20.5(18.1)
240	10	23.5(21.0)	23.2(20.9)	23.1(20.7)	22.9(20.4)	22.5(20.2)	22.1(19.7)	21.5(19.4)	20.9(18.6)	20.0(17.6)
120	20	23.0(20.5)	22.7(20.4)	22.6(20.2)	22.4(19.9)	22.0(19.7)	21.6(19.2)	21.0(18.9)	20.4(18.1)	19.5(17.1)
60	40	22.5(20.0)	22.2(19.9)	22.1(19.7)	21.9(19.4)	21.5(19.2)	21.1(18.7)	20.5(18.4)	19.9(17.6)	19.0(16.6)
48	50	22.3(19.9)	22.0(19.8)	21.9(19.5)	21.8(19.3)	21.3(19.0)	21.0(18.5)	20.3(18.2)	19.8(17.4)	18.8(16.5)
40	60	22.2(19.8)	21.9(19.6)	21.8(19.4)	21.6(19.1)	21.2(18.9)	20.8(18.4)	20.2(18.1)	19.6(17.3)	18.7(16.4)
30	80	22.0(19.5)	21.7(19.4)	21.6(19.2)	21.4(18.9)	21.0(18.7)	20.6(18.2)	20.0(17.9)	19.4(17.1)	18.5(16.1)
15	160	21.6(19.2)	21.3(18.6)	21.0(18.6)	21.0(18.6)	20.6(18.3)	20.3(17.8)	19.7(17.1)	18.9(16.4)	18.0(15.5)
8	300	21.1(18.7)	20.9(18.3)	20.7(18.0)	20.6(18.0)	20.2(17.6)	19.7(16.9)	19.2(16.7)	18.3(15.7)	17.5(14.9)
4	600	19.9(17.3)	19.7(17.1)	19.8(17.3)	19.6(17.0)	19.4(16.8)	19.0(16.4)	18.6(15.9)	17.9(15.4)	17.0(14.5)
2	1200	17.1(14.7)	17.1(14.8)	17.1(14.8)	17.1(14.7)	17.1(14.6)	17.0(14.6)	17.0(14.4)	16.7(14.0)	16.3(13.6)
1	2400	14.1(11.7)	14.2(11.7)	14.1(11.7)	14.1(11.7)	14.1(11.7)	14.1(11.7)	14.1(11.6)	14.1(11.5)	14.1(11.5)

Post Filters, SINC3 and Chop Disabled

Table 43. ADC Noise in µVRMS (µVPP) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Data Rate (SPS)	PGA GAIN								
	1	2	4	8	16	32	64	128	256
16.67	1.60(7.13)	1.05(4.14)	0.607(2.59)	0.334(1.48)	0.203(0.872)	0.142(0.622)	0.105(0.478)	0.088(0.367)	0.080(0.371)
20	1.76(7.91)	1.13(4.75)	0.647(2.75)	0.357(1.60)	0.218(1.02)	0.148(0.664)	0.112(0.492)	0.092(0.429)	0.083(0.378)
25	2.04(9.50)	1.24(5.34)	0.693(3.11)	0.409(1.75)	0.255(1.18)	0.154(0.722)	0.121(0.560)	0.101(0.456)	0.089(0.415)
27.27	2.25(10.4)	1.34(6.08)	0.707(3.29)	0.433(1.99)	0.277(1.21)	0.168(0.817)	0.132(0.617)	0.111(0.488)	0.099(0.449)

Table 44. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Data Rate (SPS)	PGA GAIN								
	1	2	4	8	16	32	64	128	256
16.67	21.6(19.4)	21.2(19.2)	21.0(18.9)	20.8(18.7)	20.6(18.5)	20.1(17.9)	19.5(17.3)	18.8(16.7)	17.9(15.7)
20	21.4(19.3)	21.1(19.0)	20.9(18.8)	20.7(18.6)	20.5(18.2)	20.0(17.8)	19.4(17.3)	18.7(16.5)	17.8(15.7)
25	21.2(19.0)	20.9(18.8)	20.8(18.6)	20.5(18.4)	20.2(18.0)	20.0(17.7)	19.3(17.1)	18.6(16.4)	17.7(15.5)
27.27	21.1(18.9)	20.8(18.6)	20.8(18.5)	20.5(18.3)	20.1(18.0)	19.8(17.5)	19.2(16.9)	18.4(16.3)	17.6(15.4)

Fast Settling, Average=16, SINC4 and Chop Disabled

Table 45. ADC Noise in µVRMS (µVPP) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
96	3.125	0.606(3.06)	0.356(1.71)	0.204(0.991)	0.113(0.573)	0.074(0.357)	0.052(0.244)	0.038(0.180)	0.030(0.146)	0.027(0.143)
30	10	1.08(5.47)	0.636(3.05)	0.364(1.77)	0.202(1.02)	0.132(0.639)	0.093(0.436)	0.068(0.321)	0.054(0.261)	0.049(0.255)
6	50	2.42(12.2)	1.42(6.83)	0.815(3.96)	0.452(2.29)	0.295(1.43)	0.208(0.975)	0.152(0.719)	0.120(0.584)	0.109(0.571)
5	60	2.54(12.6)	1.56(7.62)	0.871(4.55)	0.514(2.57)	0.314(1.56)	0.223(1.12)	0.169(0.794)	0.138(0.648)	0.119(0.682)
2	150	4.10(23.5)	2.30(10.4)	1.38(6.98)	0.802(4.08)	0.474(2.30)	0.311(1.79)	0.240(1.49)	0.222(1.29)	0.206(1.07)
1	300	6.14(33.9)	3.47(19.0)	2.07(13.1)	1.16(6.53)	0.671(3.73)	0.475(2.64)	0.410(2.60)	0.306(1.78)	0.278(1.55)

Table 46. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC4 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
96	3.125	23.0(20.6)	22.7(20.5)	22.5(20.3)	22.4(20.1)	22.0(19.7)	21.5(19.3)	21.0(18.7)	20.3(18.0)	19.4(17.1)
30	10	22.1(19.8)	21.9(19.6)	21.7(19.4)	21.6(19.2)	21.2(18.9)	20.7(18.5)	20.1(17.9)	19.5(17.2)	18.6(16.2)
6	50	21.0(18.6)	20.7(18.5)	20.5(18.3)	20.4(18.1)	20.0(17.7)	19.5(17.3)	19.0(16.7)	18.3(16.0)	17.4(15.1)
5	60	20.9(18.6)	20.6(18.3)	20.5(18.1)	20.2(17.9)	19.9(17.6)	19.4(17.1)	18.8(16.6)	18.1(15.9)	17.3(14.8)
2	150	20.2(17.7)	20.1(17.9)	19.8(17.5)	19.6(17.2)	19.3(17.1)	18.9(16.4)	18.3(15.7)	17.4(14.9)	16.5(14.2)
1	300	19.6(17.2)	19.5(17.0)	19.2(16.5)	19.0(16.5)	18.8(16.4)	18.3(15.9)	17.5(14.9)	17.0(14.4)	16.1(13.6)

Fast Settling, Average=16, SINC3 and Chop Disabled

Table 47. ADC Noise in µVRMS (µVPP) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
96	3.125	0.647(3.15)	0.367(1.73)	0.205(1.02)	0.117(0.585)	0.074(0.371)	0.053(0.247)	0.040(0.182)	0.031(0.147)	0.028(0.150)
30	10	1.16(5.63)	0.656(3.10)	0.367(1.83)	0.210(1.05)	0.132(0.664)	0.096(0.443)	0.071(0.326)	0.056(0.262)	0.051(0.268)
6	50	2.59(12.6)	1.47(6.94)	0.820(4.08)	0.469(2.34)	0.295(1.49)	0.214(0.990)	0.160(0.730)	0.124(0.586)	0.114(0.599)
5	60	2.63(13.1)	1.58(7.87)	0.884(4.64)	0.517(2.56)	0.315(1.61)	0.232(1.14)	0.174(0.838)	0.144(0.658)	0.122(0.684)
2	150	5.13(30.9)	3.14(17.2)	1.59(8.91)	0.912(5.20)	0.566(2.78)	0.364(2.23)	0.275(1.51)	0.245(1.29)	0.211(1.18)
1	300	29.0(154)	14.2(83.2)	6.99(41.6)	3.24(17.8)	1.95(11.1)	0.961(4.83)	0.558(3.16)	0.365(1.95)	0.338(1.91)

Table 48. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 3 V, V_{REF} = 2.5 V, SINC3 Filter, Chop Disabled

Filter Word	Data Rate (SPS)	PGA GAIN								
		1	2	4	8	16	32	64	128	256
96	3.125	22.9(20.6)	22.7(20.5)	22.5(20.2)	22.3(20.0)	22.0(19.7)	21.5(19.3)	20.9(18.7)	20.3(18.0)	19.4(17.0)
30	10	22.0(19.8)	21.9(19.6)	21.7(19.4)	21.5(19.2)	21.2(18.8)	20.6(18.4)	20.1(17.9)	19.4(17.2)	18.5(16.2)
6	50	20.9(18.6)	20.7(18.5)	20.5(18.2)	20.3(18.0)	20.0(17.7)	19.5(17.3)	18.9(16.7)	18.3(16.0)	17.4(15.0)
5	60	20.9(18.5)	20.6(18.3)	20.4(18.0)	20.2(17.9)	19.9(17.6)	19.4(17.1)	18.8(16.5)	18.0(15.9)	17.3(14.8)
2	150	19.9(17.3)	19.6(17.1)	19.6(17.1)	19.4(16.9)	19.1(16.8)	18.7(16.1)	18.1(15.7)	17.3(14.9)	16.5(14.0)
1	300	17.4(15.0)	17.4(14.9)	17.4(14.9)	17.6(15.1)	17.3(14.8)	17.3(15.0)	17.1(14.6)	16.7(14.3)	15.8(13.3)

ON-CHIP REGISTER MAPS

There are total 57 registers inside the device which is 8-bit, 16-bit, or 24-bit wide. These registers are used to configure and control the ADC to the desired mode of operation. These registers can be accessed through the SPI-compatible serial interface by using register read and write commands. At power-on or reset, the registers default to their initial settings, as shown in the *Reset Value* column of Table 49.

Table 49. Register map

ADDR[5:0]	NAME	DIR.	RESET VALUE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x00	STATUS	R/W	0x00	DRDYn	ERR	0	POR_FLAG	CH_ACTIVE[3:0]			
0x01	ADC_CTRL	R/W	0x0000	0	0	0	NU	CONT_READ	DATUS	NU	REF_EN
				POWER MODE[1:0]		MODE[3:0]				CLK_SEL[1:0]	
0x02	DATA	R	0x000000	DATA[23:16]							
				DATA[15:8]							
				DATA[7:0]							
0x03	IO1_CTRL	R/W	0x000000	GPIO_DAT4	GPIO_DAT3	GPIO_DAT2	GPIO_DAT1	GPIO_CTRL4	GPIO_CTRL3	GPIO_CTRL2	GPIO_CTRL1
				PDSW	IDAC_PAIR	IOUT1[2:0]			IOUT0[2:0]		
				IOUT1_CH[3:0]				IOUT0_CH[3:0]			
0x04	IO2_CTRL	R/W	0x0000	VBIAS15	VBIAS14	VBIAS13	VBIAS12	VBIAS11	VBIAS10	VBIAS9	VBIAS8
				VBIAS7	VBIAS6	VBIAS5	VBIAS4	VBIAS3	VBIAS2	VBIAS1	VBIAS0
0x05	ID	R	0x14/0x16	0	0	0	1	0	1	B-Version	0
0x06	ERR	R	0x000000	0	0	0	0	0	ADC_CAL_ERR	0	ADC_SAT_ERR
				0	0	0	0	REF_DET_ERR	0	0	0
				0	0	SPI_CNT_ERR	SPI_RD_ERR	SPI_WR_ERR	SPI_CRC_ERR	0	0
0x07	ERR_EN	R/W	0x000040	0	0	0	0	0	ADC_CAL_ERR_EN	0	ADC_SAT_ERR_EN
				0	0	0	0	REF_DET_EN	0	0	0
				0	1	SPI_CNT_ERR_EN	SPI_RD_ERR_EN	SPI_WR_ERR_EN	SPI_CRC_EN	0	0
0x08	MCLK_CNT	R	0x00	MCLK_CNT[7:0]							
0x09	CHAN0	R/W	0x8001	ENABLE	SETUP[2:0]			IOUT_OFF	0	AINP[4:3]	
				AINP[2:0]			AINN[4:0]				
0x0A	CHAN1	R/W	0x0001	CHAN1[15:0]							
0x0B	CHAN2	R/W	0x0001	CHAN2[15:0]							
0x0C	CHAN3	R/W	0x0001	CHAN3[15:0]							
0x0D	CHAN4	R/W	0x0001	CHAN4[15:0]							
0x0E	CHAN5	R/W	0x0001	CHAN5[15:0]							
0x0F	CHAN6	R/W	0x0001	CHAN6[15:0]							
0x10	CHAN7	R/W	0x0001	CHAN7[15:0]							
0x11	CHAN8	R/W	0x0001	CHAN8[15:0]							
0x12	CHAN9	R/W	0x0001	CHAN9[15:0]							
0x13	CHAN10	R/W	0x0001	CHAN10[15:0]							
0x14	CHAN11	R/W	0x0001	CHAN11[15:0]							
0x15	CHAN12	R/W	0x0001	CHAN12[15:0]							
0x16	CHAN13	R/W	0x0001	CHAN13[15:0]							
0x17	CHAN14	R/W	0x0001	CHAN14[15:0]							
0x18	CHAN15	R/W	0x0001	CHAN15[15:0]							
0x19	CONF0	R/W	0x0860	0	0	0	PGA[3]	BIPOLAR	BURNOUT[1:0]		NU
				NU	AIN_BUF	AIN_BUF	REF_SEL[1:0]		PGA[2:0]		
0x1A	CONF1	R/W	0x0860	CONF1[15:0]							
0x1B	CONF2	R/W	0x0860	CONF2[15:0]							
0x1C	CONF3	R/W	0x0860	CONF3[15:0]							
0x1D	CONF4	R/W	0x0860	CONF4[15:0]							
0x1E	CONF5	R/W	0x0860	CONF5[15:0]							
0x1F	CONF6	R/W	0x0860	CONF6[15:0]							
0x20	CONF7	R/W	0x0860	CONF7[15:0]							
0x21	FILT0	R/W	0x060180	FILTER[2:0]			REJ60	POST_FILTER[2:0]			LATENCY
				DELAY[3:0]				CHOP	FS[10:8]		
				FS[7:0]							
0x22	FILT1	R/W	0x060180	FILT1[23:0]							
0x23	FILT2	R/W	0x060180	FILT2[23:0]							
0x24	FILT3	R/W	0x060180	FILT3[23:0]							
0x25	FILT4	R/W	0x060180	FILT4[23:0]							
0x26	FILT5	R/W	0x060180	FILT5[23:0]							

0x27	FILT6	R/W	0x060180	FILT6[23:0]
0x28	FILT7	R/W	0x060180	FILT7[23:0]
0x29	OFFSET0	R/W	0x800000	OFFSET0[23:16]
				OFFSET0[15:8]
				OFFSET0[7:0]
0x2A	OFFSET1	R/W	0x800000	OFFSET1[23:0]
0x2B	OFFSET2	R/W	0x800000	OFFSET2[23:0]
0x2C	OFFSET3	R/W	0x800000	OFFSET3[23:0]
0x2D	OFFSET4	R/W	0x800000	OFFSET4[23:0]
0x2E	OFFSET5	R/W	0x800000	OFFSET5[23:0]
0x2F	OFFSET6	R/W	0x800000	OFFSET6[23:0]
0x30	OFFSET7	R/W	0x800000	OFFSET7[23:0]
0x31	GAIN0	R/W	0x555555	GAIN0[23:16]
				GAIN0[15:8]
				GAIN0[7:0]
0x32	GAIN1	R/W	0x555555	GAIN1[23:0]
0x33	GAIN2	R/W	0x555555	GAIN2[23:0]
0x34	GAIN3	R/W	0x555555	GAIN3[23:0]
0x35	GAIN4	R/W	0x555555	GAIN4[23:0]
0x36	GAIN5	R/W	0x555555	GAIN5[23:0]
0x37	GAIN6	R/W	0x555555	GAIN6[23:0]
0x38	GAIN7	R/W	0x555555	GAIN7[23:0]

STATUS Register

Table 50. STATUS Register (Address = 0x00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DRDYn	ERR	0	POR_FLAG	CHD[3:0]			

Power-On/Reset Value = 0x00

Bits	Bit Name	Access	Reset	Description
7	DRDYn	R	1'b1	**ADC Ready Bit:** This bit is cleared when new data is written to the ADC data register. It is set automatically after the ADC data register is read. In addition to this bit, DOUT/DRDYn pin can also be used as an alternative to monitor the update of new ADC data.
6	ERR	R	1'b0	**ADC Error Bit.** This bit is written at the same time as new data update. Error sources include input overrange, input underrange, or lower than expected reference voltage. This bit is cleared by a read of the error register.
5	Reserved	R	1'b0	**Reserved**
4	POR_FLAG	R	1'b0	**Power-On Reset Flag:** The bit indicates while a power-on reset occurs. A power-on reset occurs on power-up while the power supply voltage goes below a threshold voltage, while reset is preformed, and when coming out of power-down mode. The status register must be read to clear the bit.
3:0	CHD[3:0]	R	4'b0000	**Data Channel Number:** These bits indicate the corresponding channel to the ADC data in data register. **0000:** Channel 0 **0001:** Channel 1 **0010:** Channel 2 **0011:** Channel 3 **0100:** Channel 4 **0101:** Channel 5 **0110:** Channel 6 **0111:** Channel 7 **1000:** Channel 8 **1001:** Channel 9 **1010:** Channel 10

1011: Channel 11
1100: Channel 12
1101: Channel 13
1110: Channel 14
1111: Channel 15

ADC_CTRL Register

Table 51. ADC_CTRL Register (Address = 0x01)

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	NU	CONT_READ	DATUS	NU	REF_EN
POWER MODE[1:0]		MODE[3:0]				CLK_SEL[1:0]	

Power-On/Reset Value = 0x0000

Bits	Bit Name	Access	Reset	Description
15:13	RESERVED	R/W	3'b000	**Reserved** Always write 3'b000
12	NU	R/W	1'b0	**Not Used**
11	CONT_READ	R/W	1'b0	**Continuous Read Enable Bit:** When this bit is set to 1, the device is placed in continuous data read mode and the contents of the data register are automatically placed on the DOUT/DRDY pin when SCLK pulses are applied after the DOUT/DRDY pin goes low to indicate that a conversion is complete. Register read or write command is not functioning in continuous data read mode. To exit continuous data read mode, send a data read by register command (0x42).
10	DATUS	R/W	1'b0	**Status Enable Bit:** When DATUS is set to 1, the contents of the status register are transmitted along with each data register read.
9	NU	R/W	1'b0	**Not Used**
8	REF_EN	R/W	1'b0	**Internal Reference Enable Bit:** While this bit is enabled, the 2.5V internal reference is enabled and available at the REFOUT pin. 0: Off (default) 1: On
7:6	POWER MODE[1:0]	R/W	2'b00	**Power Mode Select Bits:** These bits select the power mode. The current consumption and output data rate ranges are dependent on the power mode. 00: Low power (default) 01: Middle1 power 10: Middle2 power 11: Full Power
5:2	MODE[3:0]	R/W	4'b0000	**Mode Select Bits:** These bits select the operating mode of the device. 0000: Continuous conversion mode. (default) 0001: Single conversion mode. ADC first wakeup if in idle or sleep mode; resets the filter to perform one conversion; and enters standby mode. The conversion result remains in the data register with DOUT/DRDYn as low. 0010: Standby mode. All circuitry is turned off except the internal LDO. 0011: Sleep mode. Most of circuitry is turned off to save the power. PSW pin connection remains active in sleep mode. 0100: Idle mode. The digital filter is in reset state with ADC free running. 0101: Internal zero-scale calibration. 0110: Internal full-scale calibration. 0111: System zero-scale calibration. 1000: System full-scale calibration. For each above calibration mode, DOUT/DRDYn goes high when the calibration is initiated and returns low when the calibration is complete.

				The ADC is automatically placed in idle mode after the calibration. The measured offset/full-scale coefficient is placed in the offset/full-scale register of the selected channel.
1:0	CLK_SEL[1:0]	R/W	2'b10	**Clock Select Bits:** These bits select the clock source for the ADC. 00: Internal clock with CLK tristated. (default) 01: Internal clock with its output on CLK pin. 10: External clock applied to the CLK pin. 11: External clock applied to the CLK pin.

DATA Register

The conversion result from the ADC is store in this data register. This is a read-only register. On completion of a read operation from this register, the DOUT/DRDYn bit/pin is set to logic 1.

Table 52. DATA Register (Address = 0x02)

BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT18	BIT 17	BIT 16
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DATA[23]	DATA[22]	DATA[21]	DATA[20]	DATA[19]	DATA[18]	DATA[17]	DATA[16]
DATA[15]	DATA[14]	DATA[13]	DATA[12]	DATA[11]	DATA[10]	DATA[9]	DATA[8]
DATA[7]	DATA[6]	DATA[5]	DATA[4]	DATA[3]	DATA[2]	DATA[1]	DATA[0]

Power-On/Reset Value = 0x000000

Bits	Bit Name	Access	Reset	Description
23:0	DATA[23:0]	R	0x000000	**Data Bits:** The 24-bit word is signed number in 2's complement format. See Data Format section for more information.

IO1_CNTL Register

Table 53. IO1_CNTL Register (Address = 0x03)

BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT18	BIT 17	BIT 16
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
GPIO_DAT4	GPIO_DAT3	GPIO_DAT2	GPIO_DAT1	GPIO_CTRL4	GPIO_CTRL3	GPIO_CTRL2	GPIO_CTRL1
PDSW	IDAC_PAIR	IOUT1[2:0]			IOUT0[2:0]		
IOUT1_CH[3:0]				IOUT02_CH[3:0]			

Power-On/Reset Value = 0x000000

Bits	Bit Name	Access	Reset	Description
23	GPIO_DAT4	R/W	1'b0	**Data Output P4 Bit:** This bit sets the value of the P4 output pin if GPIO_CTRL4 bit is set to 1. During IO1_CTRL register read, the GPIO_DAT4 reflects the status of the P4 pin if GPIO_CTRL4 bit is set to 1.
22	GPIO_DAT3	R/W	1'b0	**Data Output P3 Bit:** This bit sets the value of the P3 output pin if GPIO_CTRL3 bit is set to 1. During IO1_CTRL register read, the GPIO_DAT3 reflects the status of the P3 pin if GPIO_CTRL3 bit is set to 1.
21	GPIO_DAT2	R/W	1'b0	**Data Output P2 Bit:** This bit sets the value of the P2 output pin if GPIO_CTRL2 bit is set to 1. During IO1_CTRL register read, the GPIO_DAT2 reflects the status of the P2 pin if GPIO_CTRL2 bit is set to 1.
20	GPIO_DAT1	R/W	1'b0	**Data Output P1 Bit:** This bit sets the value of the P1 output pin if GPIO_CTRL1 bit is set to 1. During IO1_CTRL register read, the GPIO_DAT1 reflects the status of the P1 pin if GPIO_CTRL1 bit is set to 1.
19	GPIO_CTRL4	R/W	1'b0	**P4 Output Enable Bit:** When this bit is set to 1, the P4 pins is configured as output. When this bit is set to 0, the P4 pins is tri-state.

18	GPIO_CTRL3	R/W	1'b0	**P3 Output Enable Bit:** When this bit is set to 1, the P3 pins is configured as output. When this bit is set to 0, the P3 pins is tri-state.
17	GPIO_CTRL2	R/W	1'b0	**P2 Output Enable Bit:** When this bit is set to 1, the P2 pins is configured as output. When this bit is set to 0, the P2 pins is tri-state.
16	GPIO_CTRL1	R/W	1'b0	**P1 Output Enable Bit:** When this bit is set to 1, the P1 pins is configured as output. When this bit is set to 0, the P1 pins is tri-state.
15	PDSW	R/W	1'b0	**Power-down Switch Control Bit:** When this bit is set to 1, the switch is closed to short PSW to AVSS with low on-resistor of typical 3 Ohms. The switch is open if the bit is cleared. The switch remains active in standby and sleep modes.
14	IDAC_PAIR	R/W	1'b0	**IDAC PAIR Enable Bit:** Set this bit while both IOUT1 and IOUT0 are used as a pair to improve the IOUT matching and measurement accuracy. 0: Disabled (default) 1: Enabled
13:11	IOUT1[2:0]	R/W	3'b000	**IOUT1 Current Bits:** These bits set the value of the excitation current source IOUT1 applied to the analog input pin. 000: Off (default) 001: 50μA 010: 100μA 011: 250μA 100: 500μA 101: 750μA 110: 1000μA 111: 1000μA
10:8	IOUT0[2:0]	R/W	3'b000	**IOUT0 Current Bits:** These bits set the value of the excitation current source IOUT0 applied to the analog input pin. 000: Off (default) 001: 50μA 010: 100μA 011: 250μA 100: 500μA 101: 750μA 110: 1000μA 111: 1000μA
7:4	IOUT1_CH[3:0]	R/W	4'b0000	**IOUT1 Channel Select Bits:** These bits select the analog input channel for the excitation current source IOUT1. 0000: AIN0 pin (default) 0001: AIN1 pin 0010: AIN2 pin 0011: AIN3 pin 0100: AIN4 pin 0101: AIN5 pin 0110: AIN6 pin 0111: AIN7 pin 1000: AIN8 pin 1001: AIN9 pin 1010: AIN10 pin 1011: AIN11 pin 1100: AIN12 pin 1101: AIN13 pin 1110: AIN14 pin 1111: AIN15 pin
3:0	IOUT0_CH[3:0]	R/W	4'b0000	**IOUT0 Channel Select Bits:** These bits select the analog input channel for the excitation current source IOUT0.

0000: AIN0 pin (default)
0001: AIN1 pin
0010: AIN2 pin
0011: AIN3 pin
0100: AIN4 pin
0101: AIN5 pin
0110: AIN6 pin
0111: AIN7 pin
1000: AIN8 pin
1001: AIN9 pin
1010: AIN10 pin
1011: AIN11 pin
1100: AIN12 pin
1101: AIN13 pin
1110: AIN14 pin
1111: AIN15 pin

IO2_CNTL Registers

This register provides the option to internally bias the analog input pins at the level of middle analog supply (AVDD+AVSS)/2. Multiple channels can be biased at the same time.

Table 54. IO2_CNTL Register (Address = 0x04)

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VBIAS[15]	VBIAS[14]	VBIAS[13]	VBIAS[12]	VBIAS[11]	VBIAS[10]	VBIAS[9]	VBIAS[8]
VBIAS[7]	VBIAS[6]	VBIAS[5]	VBIAS[4]	VBIAS[3]	VBIAS[2]	VBIAS[1]	VBIAS[0]

Power-On/Reset Value = 0x0000

Bits	Bit Name	Access	Reset	Description
15	VBIAS[15]	R/W	1'b0	**VBIAS Enable Bit:** When this bit is set to logic 1, the internal bias voltage is available on AIN15.
14	VBIAS[14]	R/W	1'b0	**VBIAS Enable Bit:** When this bit is set to logic 1, the internal bias voltage is available on AIN14.
13	VBIAS[13]	R/W	1'b0	**VBIAS Enable Bit:** When this bit is set to logic 1, the internal bias voltage is available on AIN13.
12	VBIAS[12]	R/W	1'b0	**VBIAS Enable Bit:** When this bit is set to logic 1, the internal bias voltage is available on AIN12.
11	VBIAS[11]	R/W	1'b0	**VBIAS Enable Bit:** When this bit is set to logic 1, the internal bias voltage is available on AIN11.
10	VBIAS[10]	R/W	1'b0	**VBIAS Enable Bit:** When this bit is set to logic 1, the internal bias voltage is available on AIN10.
9	VBIAS[9]	R/W	1'b0	**VBIAS Enable Bit:** When this bit is set to logic 1, the internal bias voltage is available on AIN9.
8	VBIAS[8]	R/W	1'b0	**VBIAS Enable Bit:** When this bit is set to logic 1, the internal bias voltage is available on AIN8.
7	VBIAS[7]	R/W	1'b0	**VBIAS Enable Bit:** When this bit is set to logic 1, the internal bias voltage is available on AIN7.
6	VBIAS[6]	R/W	1'b0	**VBIAS Enable Bit:** When this bit is set to logic 1, the internal bias voltage is available on AIN6.

5	VBIAS[5]	R/W	1'b0	**VBIAS Enable Bit:** When this bit is set to logic 1, the internal bias voltage is available on AIN5.
4	VBIAS[4]	R/W	1'b0	**VBIAS Enable Bit:** When this bit is set to logic 1, the internal bias voltage is available on AIN4.
3	VBIAS[3]	R/W	1'b0	**VBIAS Enable Bit:** When this bit is set to logic 1, the internal bias voltage is available on AIN3.
2	VBIAS[2]	R/W	1'b0	**VBIAS Enable Bit:** When this bit is set to logic 1, the internal bias voltage is available on AIN2.
1	VBIAS[1]	R/W	1'b0	**VBIAS Enable Bit:** When this bit is set to logic 1, the internal bias voltage is available on AIN1.
0	VBIAS[0]	R/W	1'b0	**VBIAS Enable Bit:** When this bit is set to logic 1, the internal bias voltage is available on AIN0.

ID Register

Table 55. ID Register (Address = 0x05)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	1	0	1	B-Version	0

Power-On/Reset Value = 0x14(SIG7128)/0x16(SIG7128B)

Bits	Bit Name	Access	Reset	Description
7:0	ID	R	8'b000101x0	**ID Bits:** Read only. SIG7128: 0x14 SIG7128B: 0x16

ERR Register

Table 56. ERR Register (Address = 0x06)

BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT18	BIT 17	BIT 16
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	ADC_CAL_ERR	0	ADC_SAT_ERR
0	0	0	0	REF_DET_ERR	0	0	0
0	0	SPI_CNT_ERR	SPI_RD_ERR	SPI_WR_ERR	SPI_CRC_ERR	0	0

Power-On/Reset Value = 0x000000

Bits	Bit Name	Access	Reset	Description
23:19	RESERVED	R	5'b00000	**Reserved**
18	ADC_CAL_ERR	R	1'b0	**ADC CAL Flag:** This flag is set if an error occurs during a calibration.
17	RESERVED	R	1'b0	**Reserved**
16	ADC_SAT_ERR	R	1'b0	**ADC SAT Flag:** This flag is set if the modulator is saturated during a conversion.
15:11	RESERVED	R	4'b0000	**Reserved**
11	REF_DET_ERR	R	1'b0	**Reference Detection Flag:** This flag indicates when the reference input voltage is less than specified threshold, which is about 0.4V.
10:6	RESERVED	R	5'b00000	**Reserved**
5	SPI_CNT_ERR	R	1'b0	**SPI CLK Count Flag:** This flag is set when the number of SCLK cycles is not multiple of eight during CSn pin as low.

4	SPI_RD_ERR	R	1'b0	**SPI Read Flag:** This flag is set if an error occurs during an SPI read operation.
3	SPI_WR_ERR	R	1'b0	**SPI Write Flag:** This flag is set if an error occurs during an SPI Write operation.
2	SPI_CRC_ERR	R	1'b0	**SPI CRC Flag:** This flag is set if an error occurs in the CRC check of the serial communication.
1:0	RESERVED	R	2'b00	**Reserved**

ERR_EN Register

Table 57. ERR_EN Register (Address = 0x07)

BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT18	BIT 17	BIT 16
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	MCLK_CNT_EN	0	0	0	ADC_CAL_ERR_EN	0	ADC_SAT_ERR_EN
0	0	0	0	REF_DET_ERR_EN	0	0	0
0	1	SPI_CNT_ERR_EN	SPI_RD_ERR_EN	SPI_WR_ERR_EN	SPI_CRC_ERR_EN	0	0

Power-On/Reset Value = 0x000040

Bits	Bit Name	Access	Reset	Description
23	RESERVED	R/W	1'b0	**Reserved** Always write 1'b0
22	MCLK_CNT_EN	R/W	1'b0	**Master Clock Counter:** When this flag is set, the master clock counter is enabled and the result is reported via MCLK_COUNT Register.
21:19	RESERVED	R/W	3'b000	**Reserved** Always write 3'b000
18	ADC_CAL_ERR_EN	R/W	1'b0	**ADC CAL Flag:** This flag is set if an error occurs during a calibration.
17	RESERVED	R/W	1'b0	**Reserved** Always write 1'b0
16	ADC_SAT_ERR_EN	R/W	1'b0	**ADC SAT Flag:** This flag is set if the modulator is saturated during a conversion.
15:11	RESERVED	R/W	4'b0000	**Reserved** Always write 4'b0000
11	REF_DET_ERR_EN	R/W	1'b0	**Reference Detection Enable Bit:** When this bit is enabled, the REF_DET_ERR bit in the ERR Register indicates when the reference input voltage is less than specified threshold, which is about 0.4V.
10:6	RESERVED	R/W	5'b00001	**Reserved** Always write 5'b00001
5	SPI_CNT_ERR_EN	R/W	1'b0	**SPI CLK Count Enable Bit:** When this bit is set to 1, the SCLK counter is enabled. All read and write operations to the ADC are multiples of eight bits. For every serial communication, the SCLK counter counts the number of SCLK pulses. CSn must be used to frame each read and write operation. If the number of SCLK pulses used during a communication is not a multiple of eight, the SPI_CNT_ERR bit in the ERR Register is set.
4	SPI_RD_ERR_EN	R/W	1'b0	**SPI Read Enable Bit:** When this bit is set to1, the SPI_RD_ERR bit in the ERR register is set when an error occurs during a read operation. CSn must be used to frame each read operation.
3	SPI_WR_ERR_EN	R/W	1'b0	**SPI Write Enable Bit:** When this bit is set to1, the SPI_WR_ERR bit in the ERR Register is set when an error occurs during a write operation. CSn must be used to frame each write operation.

2	SPI_CRC_ERR_EN	R/W	1'b0	**SPI CRC Enable Bit:** This bit enables a CRC check of all read and write operations. The SPI_CRC_ERR bit in the ERR Register is set if the CRC check fails. In addition, an 8-bit CRC word is appended to all data read
1:0	RESERVED	R/W	2'b00	**Reserved** Always write 2'b00

MCLK_CNT Register

Table 58. MCLK_CNT Register (Address = 0x08)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MCLK_CNT[7:0]							

Power-On/Reset Value = 0x00

Bits	Bit Name	Access	Reset	Description
7:0	MCLK_CNT	R	8'b00000000	**MCLK Counter Bits:** Read only. These bits allows the user to determine the frequency of internal/external oscillator. Internally, a clock counter increments every 131 pulses of the sampling clock (614.4kHz in full power mode, 307.2kHz in mid2 power mode, 153.6kHz in mid1 power mode and 76.8kHz in low power mode). The 8-bits counter wraps around on reaching its maximum value.

CHANx Registers

The device has total sixteen configuration registers with names from CHAN0 to CHAN15.

Table 59. CHANx Register (Address = 0x09 - 0x18)

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ENABLE	SETUP[2:0]			IOUT_OFF	0	AINP[4:3]	
AINP[2:0]			AINN[4:0]				

Power-On/Reset Value = 0x8001(CHAN0)/0x0001(CHAN1-CHAN15)

Bits	Bit Name	Access	Reset	Description
15	ENABLE	R/W	1'bx	**Channel Enable Bit:** When this bit is enabled, this channel is enabled for the conversion sequence. By default, only the enable bit for Channel 0 is set. The order of conversions starts with the lowest enabled channel, then cycles through successively higher channel numbers, before wrapping around to the lowest channel again. When the ADC writes a result for a particular channel, the four LSBs of the STATUS Register are set to the channel number, 0 to 15. When the DATUS bit in the ADC_CNTL Register is set, the contents of the status register are appended to each conversion when it is read. Use this function when several channels are enabled to determine the corresponding channel information of the conversion data.
14:12	SETUP[2:0]	R/W	3'b000	**Setup Select Bits:** These bits identify which of the eight setups are used to configure the ADC for this channel. A setup comprises a set of four registers: analog configuration, output data rate/filter selection, offset register, and gain register. 000: CONF0/FILT0/OFFSET0/GAIN0 (default) 001: CONF1/FILT1/OFFSET1/GAIN1 010: CONF2/FILT2/OFFSET2/GAIN2 011: CONF3/FILT3/OFFSET3/GAIN3 100: CONF4/FILT4/OFFSET4/GAIN4 101: CONF5/FILT5/OFFSET5/GAIN5 110: CONF6/FILT6/OFFSET6/GAIN6 111: CONF7/FILT7/OFFSET7/GAIN7
11	IOUT_OFF	R/W	1'b1	**IOUT Disable Bit:** When this bit is set to 1, the excitation current sources are forced to off disregarding the configuration in IO1_CNTL Register.

10	RESERVED	R/W	1'b0	**Reserved** Always write 1'b0
9:5	AINP[4:0]	R/W	5'b00000	**Positive Input AINP Select Bits:** Select the positive input connection. 00000: AIN0 (default) 00001: AIN1 00010: AIN2 00011: AIN3 00100: AIN4 00101: AIN5 00110: AIN6 00111: AIN7 01000: AIN8 01001: AIN9 01010: AIN10 01011: AIN11 01100: AIN12 01101: AIN13 01110: AIN14 01111: AIN15 10000: Temp Sensor+ 10001: AVSS 10010: Internal reference 10011: DGND 10100: (AVDD-AVSS)/6+ 10101: (AVDD-AVSS)/6- 10110: (IOVDD-DGND)/6+ 10111: (IOVDD-DGND)/6- 11000: Reserved 11001: Reserved 11010: Reserved 11011: Reserved 11100: V_20MV_P 11101: V_20MV_N 11110: Reserved 11111: Reserved
4:0	AINN[4:0]	R/W	5'b00001	**Negative Input AINN Select Bits:** Select the negative input connection. 00000: AIN0 00001: AIN1 (default) 00010: AIN2 00011: AIN3 00100: AIN4 00101: AIN5 00110: AIN6 00111: AIN7 01000: AIN8 01001: AIN9 01010: AIN10 01011: AIN11 01100: AIN12 01101: AIN13 01110: AIN14 01111: AIN15 10000: Temp Sensor- 10001: AVSS 10010: Internal reference 10011: DGND 10100: (AVDD-AVSS)/6+

10101: (AVDD-AVSS)/6-
10110: (IOVDD-DGND)/6+
10111: (IOVDD-DGND)/6-
11000: Reserved
11001: Reserved
11010: Reserved
11011: Reserved
11100: V_20MV_P
11101: V_20MV_N
11110: Reserved
11111: Reserved

CONFx Registers

The device has total eight configuration registers with names from CONF0 to CONF7. SETUP[2:0] bits in CHANx Registers select which conf register is used for the channel conversion.

Table 60. CONFx Register (Address = 0x19 - 0x20)

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	PGA[3]	BIPOLAR	BURNOUT[1:0]		NU
NU	AIN_BUF	AIN_BUF	REF_SEL[1:0]		PGA[2:0]		

Power-On/Reset Value = 0x0860

Bits	Bit Name	Access	Reset	Description
15:13	RESERVED	R/W	3'b000	**Reserved** Always write 3'b000
12	PGA[3]	R/W	1'b0	**PGA Gain Configuration:** Work together with PGA[2:0] bits to select the PGA gain.
11	BIPOLAR	R/W	1'b0	**Bipolar Enable Bit:** This bit sets the ADC data format. 0: Unipolar mode 1: Bipolar mode (default)
10:9	BURNOUT[1:0]	R/W	2'b00	**Burnout Select Bits:** These bits selects the magnitude of the sensor burnout detect current source. 00: Off (default) 01: 0.5μA 10: 2μA 11: 4μA
8	NU	R/W	1'b0	**Not Used**
7	NU	R/W	1'b0	**Not Used**
6	AIN_BUF	R/W	1'b1	**AIN Buffer Enable Bit:** When this bit is set, analog input is buffered. Otherwise the input buffer is bypassed. The buffer can only be disabled when the gain equals 1. For higher gains, the buffer is automatically enabled.
5	AIN_BUF	R/W	1'b1	**AIN Buffer Enable Bit:** When this bit is set, analog input is buffered. Otherwise the input buffer is bypassed. The buffer can only be disabled when the gain equals 1. For higher gains, the buffer is automatically enabled.
4:3	REF_SEL[1:0]	R/W	2'b00	**Reference Select Bits:** Select the reference source for the ADC. 00: REF1+, REF1- (default) 01: REF2+, REF2- 10: 2.5V internal reference 11: AVDD

2:0	PGA[2:0]	R/W	3'b000	**PGA Gain Configuration:** Work together with PGA[3] bit to select the PGA gain. 0000: Gain=1 (default) 0001: Gain=2 0010: Gain=4 0011: Gain=8 0100: Gain=16 0101: Gain=32 0110: Gain=64 0111: Gain=128 1000: Gain=256 Others: Reserved

FILTx Registers

The device has total eight configuration registers with names from FILT0 to FILT7. SETUP[2:0] bits in CHANx Registers select which conf register is used for the channel conversion.

Table 61. FILTx Register (Address = 0x21 - 0x28)

BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT18	BIT 17	BIT 16
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FILTER[2:0]			REJ60	POST_FILTER[2:0]			LATENCY
DELAY[3:0]				CHOP	FS[10:8]		
FS[7:0]							

Power-On/Reset Value = 0x060180

Bits	Bit Name	Access	Reset	Description
23:21	FILTER[2:0]	R/W	3'b000	**Filter Select Bits:** There bits select the filter type. 000: SINC4 filter (default) 001: Reserved 010: SINC3 filter 011: Reserved 100: SINC4/SINC1 filter. The SINC4 filter is followed by an average SINC1 block. In full power and mid power modes, averaging by 16 occurs whereas averaging by 8 occurs in low power mode. 101: SINC3/SINC1 filter. The SINC3 filter is followed by an average SINC1 block. In full power and mid power modes, averaging by 16 occurs whereas averaging by 8 occurs in low power mode. 110: SINC4/post filter enabled. This device provides several post filters followed after SINC4 filter, selectable using POST_FILTER[2:0] bits. These filters offer excellent 50Hz and 60Hz rejection. 111: SINC3/post filter enabled. This device provides several post filters followed after SINC3 filter, selectable using POST_FILTER[2:0] bits. These filters offer excellent 50Hz and 60Hz rejection.
20	REJ60	R/W	1'b0	**50/60Hz Notch Bit:** This bit can only be effective while FS[10:0] is setting to have output data rate as 50SPS. A filter notch is placed at 60Hz to allow simultaneous 50Hz/60Hz rejection.
19:17	POST_FILTER[2:0]	R/W	3'b011	**Post Filter Select Bits:** There bits select the post filter type. This filter offers good 50Hz and 60Hz rejection at output data rates that have zero latency approximately.

POST_FILTER	Output Data Rate (SPS)	Rejection at 50Hz and 60Hz ± 1 Hz
000	Reserved	Not applicable
001	Reserved	Not applicable
010	27.27	47
011	25	62

100	Reserved	Not applicable
101	20	86
110	16.7	92
111	Reserved	Not applicable

16	LATENCY	R/W	1'b0	**Single Cycle Settling Bit:** When this bit is set, the ADC settles in one conversion cycle so that it functions as a zero latency ADC. When chop is disabled, fast settling mode is disabled, continuous conversion mode is selected, and LATENCY bit is set, the output data rate is Output Data Rate=MAX_SPEED/FS[10:0]/N Where N is 3 for SINC3 filter and 4 for SINC4 filter with MAX_SPEED is 19200SPS for full power mode, 9600SPS for mid2 power mode, 4800SPS for mid1 power mode and 2400SPS for low power mode.
15:12	DELAY[3:0]	R/W	4'b0000	**Conversion Delay:** Provides additional delay from conversion start to the beginning of the actual conversion. This additional delay can accommodate enough time for the analog input circuitry, such as RC filter, to be fully stable before ADC starts the conversion internally so that the 1st data after channel switch is always fully settled data. 0000: 0μs (default) 0001: 125μs 0010: 250μs 0011: 500μs 0100: 1ms 0101: 2ms 0110: 4ms 0111: 8ms 1000: 16ms 1001: 32ms 1010: 64ms 1011: 128ms 1100: 256ms 1101: 512ms 1110: 1.024s 1111: 2.048s
11	CHOP	R/W	1'b0	**Chop Enable Bit:** When this bit is enabled, the offset and offset drift of the ADC are dramatically improved with longer conversion time and settling time. For default data rate settling of 50SPS with SINC4 filter, the conversion time is 20ms and the settling time is 80ms with chop disabled. If chop is enabled, the conversion time is 80ms and the settling time is 160ms.
10:0	FS[10:0]	R/W	0x180	**Data Rate Select Bits:** The 11 bits are used to configure the ADC data rate. When chop is disabled, fast settling mode is disabled, and continuous conversion mode is selected, the output data rate is Output Data Rate=MAX_SPEED/FS[10:0] With MAX_SPEED is 19200SPS for full power mode, 9600SPS for mid2 power mode, 4800SPS for mid1 power mode and 2400SPS for low power mode.

OFFSET Registers

The device has total eight offset registers with names from OFFSET0 to OFFSET7. SETUP[2:0] bits in CHANx Registers select which offset register is used for the channel conversion. OFFSET register read and write are allowed anytime.

Table 62. OFFSET Register (Address = 0x29 - 0x30)

BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT18	BIT 17	BIT 16
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OFFSET[23]	OFFSET[22]	OFFSET[21]	OFFSET[20]	OFFSET[19]	OFFSET[18]	OFFSET[17]	OFFSET[16]
OFFSET[15]	OFFSET[14]	OFFSET[13]	OFFSET[12]	OFFSET[11]	OFFSET[10]	OFFSET[9]	OFFSET[8]
OFFSET[7]	OFFSET[6]	OFFSET[5]	OFFSET[4]	OFFSET[3]	OFFSET[2]	OFFSET[1]	OFFSET[0]

Power-On/Reset Value = 0x800000

Bits	Bit Name	Access	Reset	Description
23:0	OFFSET[23:0]	R/W	0x800000	**Offset Calibration Bits:** The 24-bit word is signed number in 2's complement format. See Calibration section for more information.

GAIN Registers

The device has total eight gain registers with names from GAIN0 to GAIN7. SETUP[2:0] bits in CHANx Registers select which gain register is used for the channel conversion. GAIN register read and write are allowed anytime.

Table 63. GAIN Register (Address = 0x31 - 0x38)

BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT18	BIT 17	BIT 16
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
GAIN[23]	GAIN[22]	GAIN[21]	GAIN[20]	GAIN[19]	GAIN[18]	GAIN[17]	GAIN[16]
GAIN[15]	GAIN[14]	GAIN[13]	GAIN[12]	GAIN[11]	GAIN[10]	GAIN[9]	GAIN[8]
GAIN[7]	GAIN[6]	GAIN[5]	GAIN[4]	GAIN[3]	GAIN[2]	GAIN[1]	GAIN[0]

Power-On/Reset Value = 0x555555

Bits	Bit Name	Access	Reset	Description
23:0	GAIN[23:0]	R/W	0x555555	**Gain Calibration Bits:** The 24-bit word is unsigned positive number in binary format. See Calibration section for more information.

REVISION HISTORY

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please contact to make sure you have the latest revision.

DATE	REVISION	CHANGE
Nov. 8, 2022		Initial release.

DISCLAIMER

Signal Micro reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

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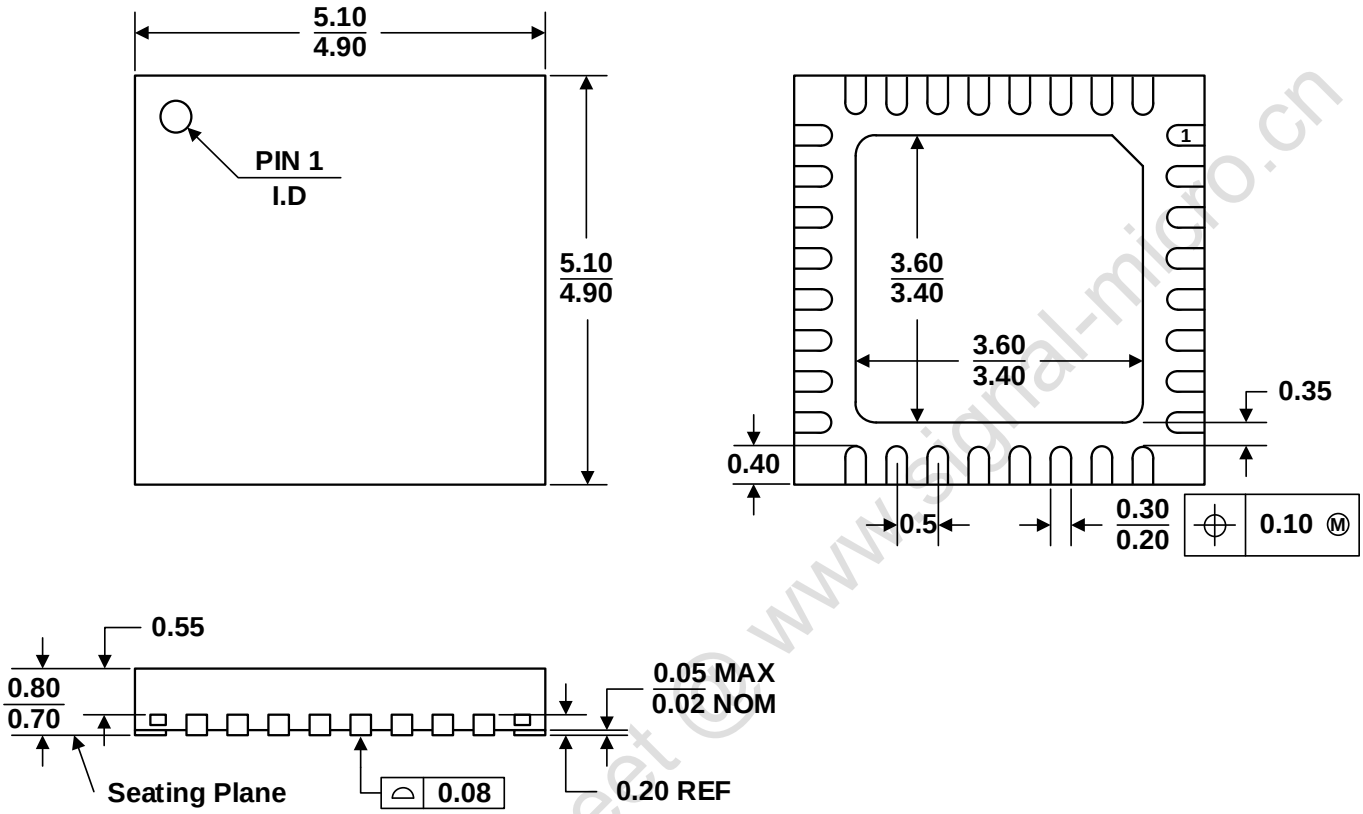
PACKAGE OUTLINE DIMENSIONS



A. Compliant to JEDEC STARDARDS MO-220.
B. All linear dimensions are in millimeters.
C. This drawing is subject to change without notice.