4-Channel 16/24-bit Sigma-Delta ADC with PGA and Reference

FEATURES

Programmable Gain: 1/2/4/8/16/32/64/128
Data Rates: 4.17SPS to 4570SPS
RMS Noise:
- **12nV at 4.17SPS (Gain=128)**
- **38nV at 16.7SPS (Gain=128)**
- **22.2 noise-free bits at 4.17SPS (Gain=1)**

Offset Drift: 5nV/°C (Gain=128)
Gain Drift: 1ppm/°C
1.17V/2.5V Internal Reference with 4ppm/°C Drift
Integral Non-Linearity: 2ppm
4 Differential Inputs
Internal or External Clock
Simultaneous 50Hz/60Hz Rejection
Reference Detect
Programmable Current Sources
On-chip Bias Voltage Generator
Burnout Current Sources
Power Supply
- **AVDD: 2.7V to 5.25V**
- **DVDD: 2.7V to 5.25V**

Current: 1.3mA
Package: 16-lead TSSOP

APPLICATIONS

Weigh Scales
Strain Gauges
Temperature Measurement
Industrial Process Control
Pressure Sensors

DESCRIPTION

The SIG8892/8893 are low noise, low drift, and high-resolution 16/24-bit analog-to-digital converter (ADC) with integrated programmable gain amplifier (PGA) and low drift on-chip voltage reference that offers high-accuracy measurement solutions for bridge sensors, thermocouples, and resistance temperature devices (RTD).

The device contains a low noise PGA with gains selected from 1, 2, 4, 8 16, 32, 64, and 128, a delta-sigma (Δ-Σ) modulator, and digital filter. A low drift 1.17V or 2.5V reference is integrated on chip and two matched excitation current sources (IEXCs) are provided for accurate RTD measurement. The output data rate from the device can be configured from 4.17SPS up to 4570SPS. 50Hz/60Hz simultaneous rejection option is also provided. Burnout current sources are provided at the analog inputs for sensor connection diagnosis.

Offset and gain calibration registers are provided with calibration command or direct register write to calibrate the ADC errors or overall system errors. SPI-compatible interface is used for device configuration.

The on-chip oscillator or an external clock can be used as the clock source to the device.

The SIG8892/8893 are available in 16-lead TSSOP packages and are fully specified over the -40°C to +125°C temperature range.

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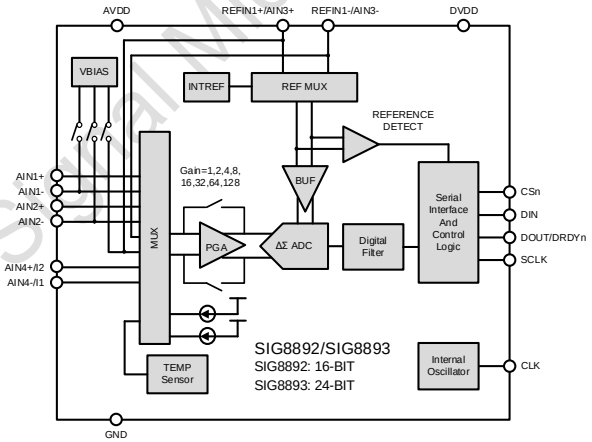
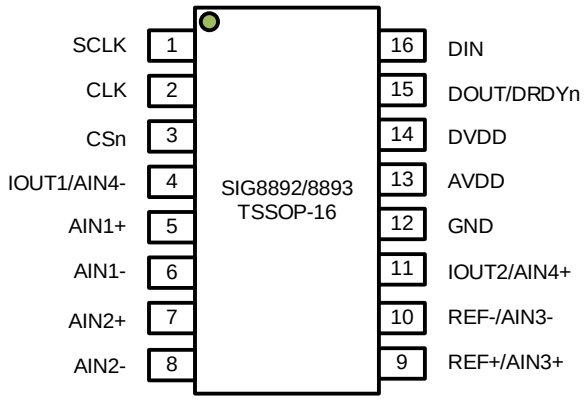
Function Block Diagram

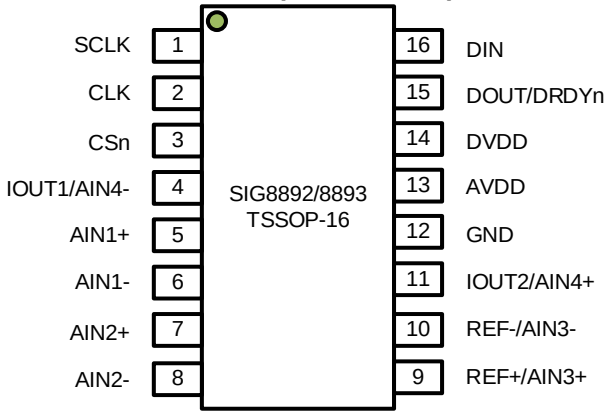


TSSOP-16



PIN CONFIGURATION and DESCRIPTIONS

TOP VIEW (Not To Scale)



PIN		FUNCTION	DESCRIPTION
NO.	NAME		
1	SCLK	Digital Input	Serial data clock.
2	CLK	Digital Input/Output	Master clock input or internal clock output depending on MODE Register bits CLK[1:0].
3	CSn	Digital Input	Serial chip select. Active low.
4	IOUT1/AIN4-	Analog Input	Internal excitation current output 1/Analog negative input channel 4.
5	AIN1+	Analog Input	Analog positive input channel 1.
6	AIN1-	Analog Input	Analog negative input channel 1.
7	AIN2+	Analog Input	Analog positive input channel 2.
8	AIN2-	Analog Input	Analog negative input channel 2.
9	REF+/AIN3+	Analog Input	Positive reference input/Analog positive input channel 3.
10	REF-/AIN3-	Analog Input	Negative reference input/Analog negative input channel 3.
11	IOUT2/AIN4+	Analog Input	Internal excitation current output 2/Analog positive input channel 4.
12	GND	Analog	Ground reference point.
13	AVDD	Analog	Positive analog power supply. 2.7V to 5.25V relative to GND. AVDD is independent of DVDD.
14	DVDD	Digital	Digital power supply, 2.7V to 5.25V. DVDD is independent of AVDD.
15	DOUT/DRDYn	Digital Output	Serial data output and data ready indicator.
16	DIN	Digital Input	Serial data input.

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PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKING OPTION
SIG8892	TSSOP-16	-40°C to +125°C	SIG8892-ITSP16-RL	Reel, 5000
SIG8893	TSSOP-16	-40°C to +125°C	SIG8893-ITSP16-RL	Reel, 5000

SPECIFICATIONS

Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
Voltage	AVDD to GND	–0.3	6.5	V
	DVDD to GND	–0.3	6.5	V
	Analog input	–0.3	V_{AVDD} + 0.3	V
	Digital input	–0.3	V_{DVDD} + 0.3	V
Current	Input current	–10	10	mA
Temperature	Junction (T_J)	–50	150	°C
	Storage (T_{stg})	-60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

SYMBOL	PARAMTER	CONDITION	VALUE	UNIT
HBM	Human-body Model	ANSI/ESDA/JEDEC JS-001	±6000	V
CDM	Charged-device model	JEDEC EIA/JS-002-2022	±2000	V

This integrated circuit can be damaged by ESD. Signal Micro recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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Electrical Characteristics

Minimum/Maximum specifications apply from -40˚C to +125˚C. Typical specifications are at +25˚C. All specification are at V_{AVDD}=5V, V_{DVDD}=3.3V, V_{GND} =0V, V_{REF}=2.5V, f_{CLK}=4.096MHz, data rate=16.7SPS, and PGA Gain=1, unless otherwise noted.

PARAMETER	TEST CONDITION OR NOTES	MIN(1)	TYP	MAX(1)	UNITS
ANALOG INPUTS					
Differential Input Voltage	$V_{IN} = V_{INP} – V_{INN}$	$–V_{REF}$/Gain		$+V_{REF}$/Gain	V
Absolute Input Voltage	Buffer Off	– 0.05		V_{AVDD} + 0.05	V
	Buffer On	+ 0.2		V_{AVDD} – 0.2	
Common Mode Input Range	Buffer On	0.2 + $\lvert V_{INMAX}\rvert$·Gain/2		V_{AVDD} – 0.2 – $\lvert V_{INMAX}\rvert$·Gain/2	V
Absolute Input Current	Buffer off		±10		nA
	Buffer On		±1		nA
SYSTEM PERFORMANCE					
PGA Gain			1/2/4/8/16/32/64/128		V/V
Resolution	SIG8893		24		Bits
	SIG8892		16		Bits
Data Rate		4.17		4570	SPS
Noise		See Noise Table			
Integral Nonlinearity (INL)	Buffer Off		±10		ppm
	Buffer On		±2		ppm
Offset Error	Chop Off		±400/Gain		µV
	Chop On		±1		µV
Offset Drift vs. Temperature	All PGA gains		±400/Gain ± 2		nV/°C
Gain Error(2)	All PGA gains	-500	±100	500	ppm
Gain Mismatch(2)	All PGA gains		150	350	ppm
Gain Drift vs. Temperature	All PGA gains	-3	±1	+3	ppm/°C
Normal Mode Rejection (NMRR)	f_{IN} = 50/60Hz, ±2%, data rate=16.7SPS		See Table 17		dB
Common Mode Rejection (CMRR)	f_{IN} = 50Hz, data rate = 470SPS	100	120		dB
Power Supply Rejection (PSRR)	AVDD	85	105		dB
	DVDD	90	110		dB
EXTERNAL REFERENCE INPUTs					
Differential Reference Voltage (V_{REF})	$V_{REF} = V_{REFP} – V_{REFN}$	0.5	2.5	V_{AVDD} + 0.1	V
Absolute Negative Reference Voltage (V_{REFN})		– 0.05		V_{REFP} – 0.5	V
Absolute Positive Reference Voltage (V_{REFP})		V_{REFN} + 0.5		V_{AVDD} + 0.05	V
Average Voltage Input Current			±4		µA
INTERNAL VOLTAGE REFERENCE					
Reference Voltage			1.17/2.5		V
Initial Accuracy(2)		-0.05%	±0.005%	+0.05%	
Temperature Drift		-20	±4	+20	ppm/°C
EXCITATION CURRENT SOURCES (IEXC1 and IEXC2)					
Output Current		10/50/100/210/250/500/1000			µA
Compliance Voltage(3)	IEXC <= 250µA	0		V_{AVDD} – 0.5	V
	IEXC = 500µA	0		V_{AVDD} – 0.6	
	IEXC = 1000µA	0		V_{AVDD} – 0.8	
Accuracy	IEXC = 10µA	-4%	±2%	+4%	
	IEXC> = 50µA	-2%	±1%	+2%	
Current Mismatch IEXC1=IEXC2	IEXC = 10µA	-3.0%	±0.60%	+3.0%	
	IEXC = 50µA	-1.5%	±0.25%	+1.5%	

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	IEXC = 100μA	-1.2%	±0.20%	+1.2%	
	IEXC = 210μA, 250μA	-1.0%	±0.18%	+1.0%	
	IEXC = 500μA	-0.8%	±0.12%	+0.8%	
	IEXC = 1000μA	-0.6%	±0.1%	+0.6%	
Temperature Drift		-90	±20	+90	ppm/°C
Temperature Drift Mismatch		-30	±5	+30	ppm/°C
Burnout Current Sources					
Current Setting			1		μA
ADC CLOCK					
External Clock	Frequency Range	2	4.096	4.1	MHz
	Duty Cycle	40%		60%	
Internal Oscillator	Nominal Frequency		4.096		MHz
	Accuracy	–3%	±0.5%	3%	
DIGITAL INPUT/OUTPUT					
High-level Output Voltage (V_{OH})	I_{OH} = 4mA	$0.8 \cdot V_{DVDD}$			V
Low-level Output Voltage (V_{OL})	I_{OL} = –4mA			$0.2 \cdot V_{DVDD}$	V
High-level Input Voltage (V_{IH})		$0.7 \cdot V_{DVDD}$		V_{DVDD}	V
Low-level Input Voltage (V_{IL})		0		$0.3 \cdot V_{DVDD}$	V
Input Hysteresis			0.5		V
Input Leakage				±10	μA
POWER SUPPLY					
AVDD Voltage (V_{AVDD})		2.7		5.25	V
DVDD Voltage (V_{DVDD})		2.7		5.25	V
AVDD Current (I_{AVDD})	Buffer Off		450	600	μA
	Buffer On		900	1200	μA
	Sleep Mode		1		μA
DVDD Current (I_{DVDD})	Active Mode		350	500	μA
	Sleep Mode		20		μA
Total Power Dissipation	Buffer Off		3.40		mW
	Buffer On		5.65		mW
	Sleep Mode		0.10		mW
TEMPERATURE RANGE					
Specified temperature range		–40		125	°C
Operating temperature range		–50		125	°C
Storage temperature range		–60		150	°C

(1) Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
(2) MIN and MAX values listed for gain error are for +25˚C room temperature only.
(3) The IDAC current does not change by more than 0.01% from the nominal value when staying within the specified compliance voltage.

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Timing Requirements: Serial Interface

Over the operating ambient temperature range and DVDD = 2.7V to 5.25V, unless otherwise noted.

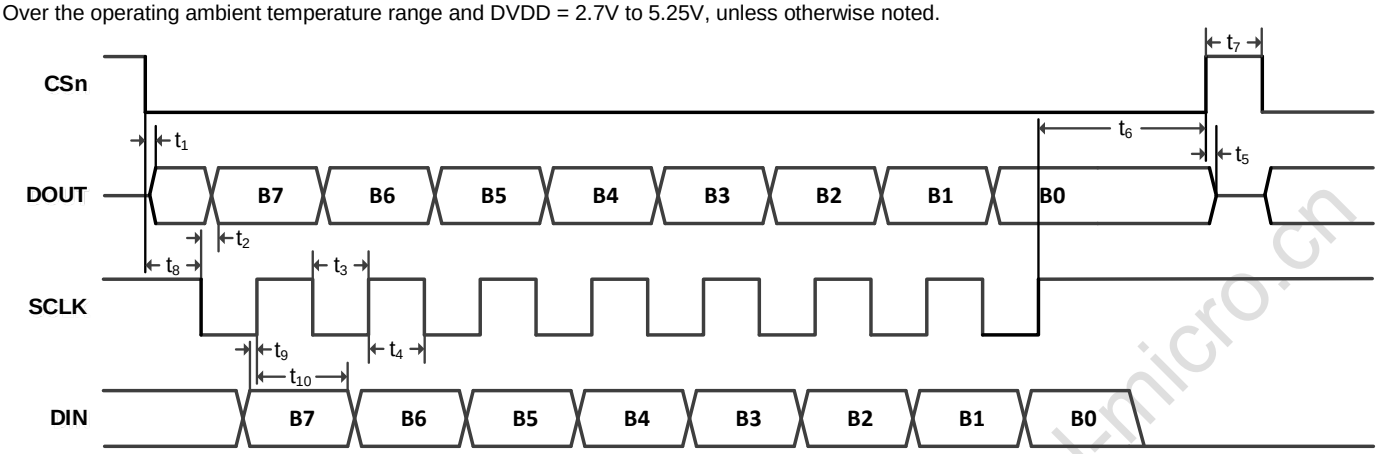

Figure 1. Serial Interface Timing Requirements

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_1	CSn falling edge to DOUT/DRDYn driven: propagation delay(1)		50	ns
t_2	SCLK falling edge to valid DOUT/DRDYn: propagation delay(1)		50	ns
t_3	SCLK low pulse width	100		ns
t_4	SCLK high pulse width	100		ns
	SCLK period	200	10^6	ns
t_5	CSn rising edge to DOUT high impedance: propagation delay		40	ns
t_6	Last SCLK rising edge to CSn rising edge: delay time	50		ns
t_7	CSn high pulse width	50		ns
t_8	CSn falling edge to first SCLK falling edge: setup time(2)	50		ns
t_9	Valid DIN to SCLK rising edge: setup time	50		ns
t_{10}	Valid DIN to SCLK rising edge: hold time	25		ns

(1) DOUT load = 20pF || 100kΩ to GND.
(2) CSn can be tied low.

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NOISE PERFORMANCE

The noise performance of the ADC is affected by PGA gain, data rate, and digital filter setting. The following tables show the rms noise and peak-to-peak noise for different data rate with chop enabled. The effective number of bits (ENOB) and noise-free bits are also listed according to Equation (1) and Equation (2):

$$\text{ENOB} = \log_2(2 \times V_{REF} / \text{Gain} / V_{RMS}) \quad (1)$$

$$\text{Noise Free Bits} = \log_2(2 \times V_{REF} / \text{Gain} / V_{p\text{-}p}) \quad (2)$$

The noise data listed in the table are typical and are generated from continuous ADC readings with differential input voltage of 0 V. With chop disabled, the noise increases by 30%.

External Reference

Table 1. ADC Noise in μVRMS (μVPP) at T_A = 25°C, V_{AVDD} = 5 V, V_{REF} = 2.5 V, Chop Enabled

FS[4:0]	Data Rate (SPS)	PGA GAIN							
		1	2	4	8	16	32	64	128
01111	4.17	0.251(1.03)	0.149(0.751)	0.099(0.493)	0.047(0.211)	0.029(0.135)	0.018(0.073)	0.016(0.073)	0.012(0.058)
01110	6.25	0.325(1.33)	0.192(0.970)	0.128(0.637)	0.060(0.273)	0.038(0.174)	0.023(0.095)	0.021(0.095)	0.016(0.074)
01101	8.33	0.398(1.63)	0.236(1.19)	0.157(0.780)	0.074(0.334)	0.046(0.213)	0.028(0.116)	0.026(0.116)	0.020(0.091)
01100	10	0.459(1.89)	0.272(1.37)	0.181(0.900)	0.085(0.386)	0.053(0.246)	0.032(0.134)	0.030(0.134)	0.023(0.105)
01011	12.5	0.562(2.31)	0.333(1.68)	0.221(1.10)	0.104(0.473)	0.065(0.302)	0.040(0.164)	0.036(0.164)	0.028(0.129)
01010	16.7	0.795(3.27)	0.471(2.38)	0.313(1.56)	0.147(0.669)	0.092(0.427)	0.056(0.232)	0.051(0.232)	0.039(0.182)
01001	16.7	0.741(3.27)	0.411(1.78)	0.279(1.41)	0.143(0.668)	0.087(0.428)	0.050(0.204)	0.049(0.213)	0.036(0.164)
01000	19.6	0.895(5.05)	0.497(2.52)	0.297(1.56)	0.166(0.728)	0.097(0.390)	0.054(0.213)	0.052(0.237)	0.043(0.200)
00111	33.2	1.01(4.75)	0.621(2.82)	0.336(1.86)	0.192(0.928)	0.120(0.538)	0.085(0.399)	0.070(0.320)	0.058(0.283)
00110	39	1.19(5.65)	0.701(3.12)	0.410(2.30)	0.230(1.04)	0.117(0.557)	0.099(0.436)	0.073(0.385)	0.065(0.298)
00101	50	1.51(7.72)	0.887(3.86)	0.497(2.15)	0.245(1.26)	0.142(0.743)	0.111(0.580)	0.070(0.390)	0.078(0.336)
00100	62	1.74(8.83)	0.959(4.31)	0.564(2.75)	0.312(1.49)	0.156(0.872)	0.133(0.622)	0.092(0.515)	0.097(0.448)
00011	125	2.35(11.6)	1.37(7.57)	0.719(3.64)	0.424(2.52)	0.268(1.50)	0.155(0.761)	0.132(0.650)	0.126(0.568)
00010	248	3.37(16.9)	2.16(12.8)	1.15(5.94)	0.660(3.75)	0.388(2.69)	0.260(1.58)	0.192(1.03)	0.154(0.898)
00001	492	4.51(30.6)	2.80(20.5)	1.57(9.50)	0.848(5.38)	0.488(3.03)	0.349(1.98)	0.282(1.67)	0.228(1.42)
00000	970	6.52(43.1)	3.91(27.0)	2.19(15.0)	1.22(7.98)	0.727(5.53)	0.481(2.92)	0.367(2.09)	0.327(2.04)
10000	1882	21.8(155)	11.3(80.0)	5.95(37.3)	2.98(21.3)	1.65(12.0)	0.918(6.86)	0.607(4.12)	0.493(3.42)
11000	2461	195(1260)	98.8(624)	47.8(315)	24.5(153)	12.4(80.1)	6.14(42.6)	3.07(19.3)	1.58(10.2)
10001	3555	221(1810)	113(826)	57.0(493)	27.8(233)	14.2(103)	7.14(57.4)	3.54(30.0)	1.83(13.6)
11001	4570	1570(11000)	779(5180)	392(2520)	194(1220)	97.0(593)	48.9(344)	24.4(159)	12.0(74.1)

Table 2. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 5 V, V_{REF} = 2.5 V, Chop Enabled

FS[4:0]	Data Rate (SPS)	PGA GAIN							
		1	2	4	8	16	32	64	128
01111	4.17	24.2(22.2)	24.0(21.7)	23.6(21.3)	23.7(21.5)	23.4(21.1)	23.1(21.0)	22.2(20.0)	21.6(19.4)
01110	6.25	23.9(21.8)	23.6(21.3)	23.2(20.9)	23.3(21.1)	23.0(20.8)	22.7(20.7)	21.8(19.7)	21.2(19.0)
01101	8.33	23.6(21.5)	23.3(21.0)	22.9(20.6)	23.0(20.8)	22.7(20.5)	22.4(20.4)	21.5(19.4)	20.9(18.7)
01100	10	23.4(21.3)	23.1(20.8)	22.7(20.4)	22.8(20.6)	22.5(20.3)	22.2(20.2)	21.3(19.2)	20.7(18.5)
01011	12.5	23.1(21.0)	22.8(20.5)	22.4(20.1)	22.5(20.3)	22.2(20.0)	21.9(19.9)	21.0(18.9)	20.4(18.2)
01010	16.7	22.6(20.5)	22.3(20.0)	21.9(19.6)	22.0(19.8)	21.7(19.5)	21.4(19.4)	20.5(18.4)	19.9(17.7)
01001	16.7	22.7(20.5)	22.5(20.4)	22.1(19.8)	22.1(19.8)	21.8(19.5)	21.6(19.5)	20.6(18.5)	20.0(17.9)
01000	19.6	22.4(19.9)	22.3(19.9)	22.0(19.6)	21.8(19.7)	21.6(19.6)	21.5(19.5)	20.5(18.3)	19.8(17.6)
00111	33.2	22.2(20.0)	21.9(19.8)	21.8(19.4)	21.6(19.4)	21.3(19.1)	20.8(18.6)	20.1(17.9)	19.4(17.1)
00110	39	22.0(19.8)	21.8(19.6)	21.5(19.1)	21.4(19.2)	21.4(19.1)	20.6(18.4)	20.0(17.6)	19.2(17.0)
00101	50	21.7(19.3)	21.4(19.3)	21.3(19.1)	21.3(18.9)	21.1(18.7)	20.4(18.0)	20.1(17.6)	18.9(16.8)
00100	62	21.5(19.1)	21.3(19.1)	21.1(18.8)	20.9(18.7)	20.9(18.5)	20.2(17.9)	19.7(17.2)	18.6(16.4)
00011	125	21.0(18.7)	20.8(18.3)	20.7(18.4)	20.5(17.9)	20.2(17.7)	19.9(17.6)	19.2(16.9)	18.2(16.1)
00010	248	20.5(18.2)	20.1(17.6)	20.0(17.7)	19.9(17.3)	19.6(16.8)	19.2(16.6)	18.6(16.2)	17.9(15.4)
00001	492	20.1(17.3)	19.8(16.9)	19.6(17.0)	19.5(16.8)	19.3(16.7)	18.8(16.3)	18.1(15.5)	17.4(14.7)
00000	970	19.5(16.8)	19.3(16.5)	19.1(16.3)	19.0(16.3)	18.7(15.8)	18.3(15.7)	17.7(15.2)	16.9(14.2)
10000	1882	17.8(15.0)	17.8(14.9)	17.7(15.0)	17.7(14.8)	17.5(14.7)	17.4(14.5)	17.0(14.2)	16.3(13.5)
11000	2461	14.6(12.0)	14.6(12.0)	14.7(12.0)	14.6(12.0)	14.6(11.9)	14.6(11.8)	14.6(12.0)	14.6(11.9)
10001	3555	14.5(11.4)	14.4(11.6)	14.4(11.3)	14.5(11.4)	14.4(11.6)	14.4(11.4)	14.4(11.3)	14.4(11.5)
11001	4570	11.6(8.8)	11.6(8.9)	11.6(9.0)	11.7(9.0)	11.7(9.0)	11.6(8.8)	11.6(8.9)	11.7(9.0)

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Internal Reference

Table 3. ADC Noise in μVRMS (μVPP) at T_A = 25°C, V_{AVDD} = 5 V, Internal 1.17V Reference, Chop Enabled

FS[4:0]	Data Rate (SPS)	PGA GAIN							
		1	2	4	8	16	32	64	128
01111	4.17	0.432(1.84)	0.207(1.09)	0.123(0.492)	0.064(0.316)	0.034(0.173)	0.022(0.097)	0.016(0.061)	0.013(0.051)
01110	6.25	0.557(2.38)	0.268(1.41)	0.159(0.635)	0.083(0.407)	0.044(0.223)	0.028(0.126)	0.020(0.079)	0.016(0.066)
01101	8.33	0.683(2.91)	0.328(1.73)	0.194(0.778)	0.101(0.499)	0.053(0.273)	0.035(0.154)	0.025(0.097)	0.020(0.081)
01100	10	0.788(3.36)	0.379(1.99)	0.225(0.899)	0.117(0.576)	0.062(0.315)	0.040(0.178)	0.029(0.112)	0.023(0.094)
01011	12.5	0.965(4.12)	0.464(2.44)	0.275(1.10)	0.143(0.706)	0.076(0.386)	0.049(0.218)	0.035(0.137)	0.028(0.115)
01010	16.7	1.37(5.82)	0.656(3.45)	0.389(1.56)	0.202(0.998)	0.107(0.546)	0.069(0.308)	0.050(0.194)	0.040(0.162)
01001	16.7	1.28(5.55)	0.756(3.26)	0.362(1.46)	0.192(0.798)	0.098(0.399)	0.061(0.238)	0.045(0.180)	0.036(0.154)
01000	19.6	1.32(6.80)	0.757(3.61)	0.362(1.70)	0.203(0.988)	0.135(0.555)	0.069(0.282)	0.070(0.310)	0.043(0.190)
00111	33.2	2.48(14.0)	1.00(4.30)	0.552(2.25)	0.254(1.13)	0.151(0.771)	0.100(0.472)	0.072(0.366)	0.068(0.309)
00110	39	2.12(9.85)	1.23(5.48)	0.553(2.50)	0.321(1.35)	0.185(0.971)	0.099(0.485)	0.080(0.405)	0.055(0.264)
00101	50	3.08(16.1)	1.49(6.93)	0.903(4.09)	0.395(1.80)	0.192(1.05)	0.136(0.745)	0.090(0.514)	0.073(0.313)
00100	62	3.25(17.3)	1.65(8.04)	3.50(24.2)	0.445(2.27)	0.255(1.16)	0.162(0.815)	0.099(0.598)	0.095(0.407)
00011	125	4.45(23.0)	2.29(11.5)	1.13(5.58)	0.589(2.58)	10400(72700)	0.199(1.11)	2600(18200)	0.117(0.599)
00010	248	6.21(36.6)	3.04(17.8)	1.66(9.95)	0.883(4.91)	0.493(2.65)	0.301(1.58)	0.197(0.993)	0.189(1.00)
00001	492	8.09(46.2)	4.72(29.5)	2.38(14.8)	1.18(8.36)	0.632(3.74)	0.392(2.25)	0.303(1.77)	0.250(1.39)
00000	970	12.2(88.5)	6.42(45.2)	3.31(20.3)	1.75(10.5)	0.947(6.09)	0.580(3.37)	0.427(2.65)	0.346(2.33)
10000	1882	19.2(127)	10.3(77.0)	5.47(39.1)	2.71(18.3)	1.45(10.3)	0.878(6.34)	0.589(4.05)	0.494(3.53)
11000	2461	92.2(606)	45.2(272)	22.6(149)	11.8(72.2)	5.87(36.7)	3.00(18.5)	1.55(9.70)	0.872(5.93)
10001	3555	105(731)	54.5(385)	26.5(194)	13.2(106)	6.72(46.8)	3.38(24.0)	1.82(13.9)	1.06(7.81)
11001	4570	728(4620)	372(2380)	187(1150)	91.3(583)	45.9(311)	23.0(136)	11.3(77.6)	5.62(35.3)

Table 4. ADC ENOB (Noise Free Bits) at T_A = 25°C, V_{AVDD} = 5 V, Internal 1.17V Reference, Chop Enabled

FS[4:0]	Data Rate (SPS)	PGA GAIN							
		1	2	4	8	16	32	64	128
01111	4.17	22.4(20.3)	22.4(20.0)	22.2(20.2)	22.1(19.8)	22.0(19.7)	21.7(19.5)	21.2(19.2)	20.5(18.4)
01110	6.25	22.0(19.9)	22.1(19.7)	21.8(19.8)	21.8(19.5)	21.7(19.3)	21.3(19.2)	20.8(18.8)	20.1(18.1)
01101	8.33	21.7(19.6)	21.8(19.4)	21.5(19.5)	21.5(19.2)	21.4(19.0)	21.0(18.9)	20.5(18.5)	19.8(17.8)
01100	10	21.5(19.4)	21.6(19.2)	21.3(19.3)	21.3(19.0)	21.2(18.8)	20.8(18.7)	20.3(18.3)	19.6(17.6)
01011	12.5	21.2(19.1)	21.3(18.9)	21.0(19.0)	21.0(18.7)	20.9(18.5)	20.5(18.4)	20.0(18.0)	19.3(17.3)
01010	16.7	20.7(18.6)	20.8(18.4)	20.5(18.5)	20.5(18.2)	20.4(18.0)	20.0(17.9)	19.5(17.5)	18.8(16.8)
01001	16.7	20.8(18.7)	20.6(18.5)	20.6(18.6)	20.5(18.5)	20.5(18.5)	20.2(18.2)	19.6(17.6)	19.0(16.9)
01000	19.6	20.8(18.4)	20.6(18.3)	20.6(18.4)	20.5(18.2)	20.0(18.0)	20.0(18.0)	19.0(16.8)	18.7(16.6)
00111	33.2	19.8(17.3)	20.2(18.1)	20.0(18.0)	20.1(18.0)	19.9(17.5)	19.5(17.2)	18.9(16.6)	18.0(15.9)
00110	39	20.1(17.9)	19.9(17.7)	20.0(17.8)	19.8(17.7)	19.6(17.2)	19.5(17.2)	18.8(16.5)	18.3(16.1)
00101	50	19.5(17.2)	19.6(17.4)	19.3(17.1)	19.5(17.3)	19.5(17.1)	19.0(16.6)	18.6(16.1)	17.9(15.8)
00100	62	19.5(17.0)	19.4(17.2)	17.4(14.6)	19.3(17.0)	19.1(16.9)	18.8(16.5)	18.5(15.9)	17.6(15.5)
00011	125	19.0(16.6)	19.0(16.6)	19.0(16.7)	18.9(16.8)	3.8(1.0)	18.5(16.0)	3.8(1.0)	17.2(14.9)
00010	248	18.5(16.0)	18.6(16.0)	18.4(15.8)	18.3(15.9)	18.2(15.8)	17.9(15.5)	17.5(15.2)	16.6(14.2)
00001	492	18.1(15.6)	17.9(15.3)	17.9(15.3)	17.9(15.1)	17.8(15.3)	17.5(15.0)	16.9(14.3)	16.2(13.7)
00000	970	17.6(14.7)	17.5(14.7)	17.4(14.8)	17.4(14.8)	17.2(14.6)	16.9(14.4)	16.4(13.8)	15.7(12.9)
10000	1882	16.9(14.2)	16.8(13.9)	16.7(13.9)	16.7(14.0)	16.6(13.8)	16.3(13.5)	15.9(13.1)	15.2(12.3)
11000	2461	14.6(11.9)	14.7(12.1)	14.7(11.9)	14.6(12.0)	14.6(12.0)	14.6(11.9)	14.5(11.9)	14.4(11.6)
10001	3555	14.4(11.6)	14.4(11.6)	14.4(11.6)	14.4(11.4)	14.4(11.6)	14.4(11.6)	14.3(11.4)	14.1(11.2)
11001	4570	11.7(9.0)	11.6(8.9)	11.6(9.0)	11.6(9.0)	11.6(8.9)	11.6(9.1)	11.7(8.9)	11.7(9.0)

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ON-CHIP REGISTER MAPS

There are total eight registers inside the device which is 8-bit, 16-bit, or 24-bit wide. These registers are used to configure and control the ADC to the desired mode of operation. These registers can be accessed through the SPI-compatible serial interface by using register read and write commands. At power-on or reset, the registers default to their initial settings, as shown in the *Reset Value* column of Table 5.

Table 5. SIG8893/SIG8892 register map

ADDR.	NAME	DIR.	RESET VALUE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
3'b000	STATUS	R	80	DRDYn	ERR	NOREF	0	24-bit	CHD[2:0]		
3'b001	MODE	R/W	000A	MD[2:0]			0	IEXC_PAIR	0	0	FAST_ST
				CLK[1:0]		FS[4]	CHOPn	FS[3:0]			
3'b010	CONFIG	R/W	0710	VBIAS[1:0]		BURN	FORMAT	0	PGA[2:0]		
				REFSEL[1:0]		REFDET	BUF	0	CH[2:0]		
3'b011	DATA	R	000000 /(0000) (1)	DATA[23:16] (SIG8893 only)							
				DATA[15:8]							
				DATA[7:0]							
3'b100	ID	R	XA/(XB)(1)	x	x	x	x	1	0	1	1/0
3'b101	IO	R/W	00	IEXCEN[2]	0	0	0	IEXCDIR[1:0]		IEXCEN[1:0]	
3'b110	OFFSET	R/W	800000 /(8000)(1)	OFFSET[23:16] (SIG8893 only)							
				OFFSET[15:8]							
				OFFSET[7:0]							
3'b111	GAIN	R/W	555555 /(5555)(1)	GAIN[23:16] (SIG8893 only)							
				GAIN[15:8]							
				GAIN[7:0]							

(1) The values in bracket are the default reset value for SIG8892.

STATUS Register

Table 6. STATUS Register (Address = 3'b000)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DRDYn	ERR	NOREF	0	24-bit	CHD[2:0]		

Power-On/Reset Value = 0x80(SIG8892)/ 0x88(SIG8893)

Bits	Bit Name	Access	Reset	Description
7	DRDYn	R	1'b1	**ADC Ready Bit:** This bit is cleared when new data is written to the ADC data register. It is set automatically after the ADC data register is read. In addition to this bit, DOUT/DRDYn pin can also be used as an alternative to monitor the update of new ADC data.
6	ERR	R	1'b0	**ADC Error Bit.** This bit is written at the same time as new data update. Error sources include input overrange, input underrange, or lower than expected reference voltage.
5	NOREF	R	1'b0	**No External Reference Bit:** The function of this bit is only enabled by setting the REFDET bit in the CONFIG Register to 1. While the REFDET bit is 1 and the selected reference voltage is below a specified threshold, which is about 0.4V, this bit is set and conversion results are clamped to all 1s.
4	RESERVED	R	1'b0	**Reserved**
3	24-bit	R	1'b0(7792) 1'b1(7793)	**24-Bit Device Indicator.** This bit indicates whether this device is 16-bit (SIG8892) or 24-bit (SIG8893).
2:0	CHD[2:0]	R	3'b000	**Data Channel Number:** These bits indicate the corresponding channel to the ADC data in data register (see Table 9).

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MODE Register

Table 7. MODE Register (Address = 3'b001)

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MD[2:0]			0	IEXC_PAIR	0	0	FAST_ST
CLK[1:0]		FS[4]	CHOPn	FS[3:0]			

Power-On/Reset Value = 0x000A

Bits	Bit Name	Access	Reset	Description
15:13	MD[2:0]	R/W	3'b000	**Mode Select Bits:** These bits select the operating mode of the device. 000: Continuous conversion mode. (default) 001: Single conversion mode. ADC first wakeup if in idle or sleep mode; resets the filter to perform one conversion; and enters sleep mode. The conversion result remains in the data register with DOUT/DRDYn as low. 010: Idle mode. The digital filter is in reset state with ADC free running. 011: Sleep mode. Most of circuitry is turned off to save the power. 100: Internal zero-scale calibration. 101: Internal full-scale calibration. 110: System zero-scale calibration. 111: System full-scale calibration. For each above calibration mode, DOUT/DRDYn goes high when the calibration is initiated and returns low when the calibration is complete. The ADC is automatically placed in idle mode after the calibration. The measured offset/full-scale coefficient is placed in the offset/full-scale register of the selected channel.
12	RESERVED	R/W	1'b0	**Reserved** Always write 1'b0
11	IEXC_PAIR	R/W	1'b0	**IEXC PAIR Enable Bit:** Set this bit while both IEXC1 and IEXC2 are used as a pair to improve the IEXC matching and measurement accuracy. 0: Disabled (default) 1: Enabled
10, 9	RESERVED	R/W	2'b00	**Reserved** Always write 2'b00
8	FAST_ST	R/W	1'b0	**Fast Startup Bit:** When FAST_ST is set, the internal bandgap stays on during sleep mode for fast startup if internal reference is selected or excitation current sources are used.
7:6	CLK[1:0]	R/W	2'b10	**Clock Select Bits:** These bits select the clock source for SYSCLK. 00: Internal 4.096MHz clock with CLK tristated. (default) 01: Internal 4.096MHz clock with its output on CLK pin. 10: External clock applied to the CLK pin. 11: External clock applied to the CLK pin.
5	FS[4]	R/W	1'b0	**Data Rate Configuration:** Selects the ADC data rate.
4	CHOPn	R/W	1'b0	**Chop Disable Bit:** When chop is enabled with bit clear to logic 0, the offset and offset drift of the ADC are dramatically improved with settling time doubled. All output data are fully settled data. For default data rate settling of 16.7SPS, the conversion time is 60ms for all output data with chop disabled. If chop is enabled, the conversion time is 120ms for the first data and 60ms thereafter.
3:0	FS[3:0]	R/W	4'b1010	**Data Rate Configuration:** Selects the ADC data rate. Here is the list of data rate corresponding to each FS[4:0] bits setting. 11001: 4570SPS 10001: 3555SPS

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11000: 2461SPS
10000: 1882SPS
00000: 970SPS
00001: 492SPS
00010: 248SPS
00011: 125SPS
00100: 62SPS
00101: 50SPS
00110: 39SPS
00111: 33.2SPS
01000: 19.6SPS
01001: 16.7SPS
01010: 16.7SPS (default)
01011: 12.5SPS
01100: 10SPS
01101: 8.33SPS
01110: 6.25SPS
01111: 4.17SPS

CONFIG Register

Table 8. CONFIG Register (Address = 3'b010)

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VBIAS[1:0]		BURN	FORMAT	0	PGA[2:0]		
REFSEL[1:0]		REFDET	BUF	0	CH[2:0]		

Power-On/Reset Value = 0x0710

Bits	Bit Name	Access	Reset	Description
15:14	VBIAS[1:0]	R/W	2'b00	**Bias Voltage Generator Enable Bits:** The negative terminal of the analog inputs can be biased at the level of middle analog supply AVDD/2. 00: Bias voltage generator disabled 01: Bias voltage connected to AIN1- 10: Bias voltage connected to AIN2- 11: Bias voltage connected to AIN3-
13	BURN	R/W	1'b0	**Burnout Enable Bit:** When this bit is enabled, a pair of 1μA current sources are applied to analog inputs to source positive input and sink negative input.
12	FORMAT	R/W	1'b0	**Data Format Bit:** This bit sets the ADC data format. 0: Bipolar mode (default) 1: Unipolar mode
11	RESERVED	R/W	1'b0	**Reserved** Always write 1'b0
10:8	PGA[2:0]	R/W	3'b111	**PGA Gain Configuration:** Selects the PGA gain. If PGA gain is set to other than 1 and 2, the BUF bit setting is ignored with buffer always enabled. 000: Gain=1 001: Gain=2 010: Gain=4 011: Gain=8 100: Gain=16 101: Gain=32 110: Gain=64 111: Gain=128 (default)

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7:6	REFSEL[1:0]	R/W	2'b00	**Reference Select Bits:** Select the reference source for the ADC. 00: REF+, REF- (default) 01: Reserved 10: 1.17V internal reference 11: 2.5V internal reference
5	REFDET	R/W	1'b0	**Reference Detection Enable Bit:** When this bit is enabled, the NOREF bit in the STATUS register indicates when the reference input voltage is less than specified threshold, which is about 0.4V.
4	BUF	R/W	1'b1	**Buffer Enable Bit:** When this bit is set, analog input is buffered. Otherwise the input buffer is bypassed. The buffer can only be disabled when the gain equals 1 or 2. For higher gains, the buffer is automatically enabled.
3	RESERVED	R/W	1'b0	**Reserved** Always write 1'b0
2:0	CH[2:0]	R/W	3'b000	**Channel Select Bits:** These bits select which channel is enabled for ADC conversion (see Table 9). When ADC finishes the conversion and places the data into data register with the corresponding channel information in STATUS register.

Table 9. Channel Selection

CHD[2:0]	Positive Input AIN+	Negative Input AIN-	Status Register Bits CHD[2:0]	Calibration Register Pair
000	AIN1+	AIN1-	000	0
001	AIN2+	AIN2-	001	1
010	AIN3+	AIN3-	010	2
011	AIN1-	AIN1-	011	0
100	AIN4+	AIN4-	100	3
101	Reserved		101	
110	Temperature Sensor(1)		110	Default Reset Values
111	AVDD Monitor(2)		111	Default Reset Values

(1) For temperature sensor measurement, PGA gain is internally forced to 1 with buffer on and internal 1.17V reference is used disregarding user register configuration.
(2) For AVDD monitor measurement, the AVDD is internally attenuated by 6, PGA gain is forced to 1 with buffer on and internal 1.17V reference is used disregarding user register configuration.

DATA Register

This register is 16 bits wide for SIG8892 and 24 bits wide for SIG8893.

Table 10. DATA Register (Address = 3'b011)

BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT18	BIT 17	BIT 16
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DATA[23]	DATA[22]	DATA[21]	DATA[20]	DATA[19]	DATA[18]	DATA[17]	DATA[16]
DATA[15]	DATA[14]	DATA[13]	DATA[12]	DATA[11]	DATA[10]	DATA[9]	DATA[8]
DATA[7]	DATA[6]	DATA[5]	DATA[4]	DATA[3]	DATA[2]	DATA[1]	DATA[0]

Power-On/Reset Value = 0x0000(SIG8892)/0x000000(SIG8893)

Bits	Bit Name	Access	Reset	Description
23:0	DATA[23:0]	R	0x000000	**Data Bits:** The 16-bit word for SIG8892 or 24-bit word for SIG8893 is signed number in 2's complement format. See Data Format section for more information.

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ID Register

Table 11. ID Register (Address = 3'b100)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
x	x	x	x	1	0	1	0/1

Power-On/Reset Value = 0xXA(SIG8892)/0xXB(SIG8893)

Bits	Bit Name	Access	Reset	Description
7:0	ID	R	8'bxxxx101x	**ID Bits:** Read only.

IO Register

Table 12. IO Register (Address = 3'b101)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IEXCEN[2]	0	0	0	IEXCDIR[1:0]		IEXCEN[1:0]	

Power-On/Reset Value = 0x00

Bits	Bit Name	Access	Reset	Description
7	IEXCEN[2]	R/W	1'b0	**IEXC Current Bit:** This bit works together with IEXCEN[1:0] to select the value of the excitation current sources applied to the analog input pins.
6, 5, 4	RESERVED	R/W	3'b000	**Reserved** Always write 3'b000
3:2	IEXCDIR[1:0]	R/W	2'b00	**Direction of Current Sources Select Bits:** 00: Current source IEXC1 connected to Pin IOUT1, Current source IEXC2 connected to Pin IOUT2. 01: Current source IEXC1 connected to Pin IOUT2, Current source IEXC2 connected to Pin IOUT1. 10: Both current source IEXC1 and IEXC2 connected to Pin IOUT1. 11: Both current source IEXC1 and IEXC2 connected to Pin IOUT2.
1:0	IEXCEN[1:0]	R/W	2'b00	**IEXC Current Bits:** Combined with IEXCEN[2], these three bits select the value of the excitation current sources applied to the analog input pins. 000: Off (default) 001: 10μA 010: 210μA 011: 1000μA 100: 50μA 101: 100μA 110: 250μA 111: 500μA

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OFFSET Register

The device has four OFFSET registers, each channel has a dedicated OFFSET register (see Table 9). This register is 16 bits wide for SIG8892 and 24 bits wide for SIG8893. OFFSET register read is allowed anytime, but writing to OFFSET register is only allowed while the device is in idle or sleep mode.

Table 13. OFFSET Register (Address = 3'b110)

BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT18	BIT 17	BIT 16
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OFFSET[23]	OFFSET[22]	OFFSET[21]	OFFSET[20]	OFFSET[19]	OFFSET[18]	OFFSET[17]	OFFSET[16]
OFFSET[15]	OFFSET[14]	OFFSET[13]	OFFSET[12]	OFFSET[11]	OFFSET[10]	OFFSET[9]	OFFSET[8]
OFFSET[7]	OFFSET[6]	OFFSET[5]	OFFSET[4]	OFFSET[3]	OFFSET[2]	OFFSET[1]	OFFSET[0]

Power-On/Reset Value = 0x8000(SIG8892)/0x800000(SIG8893)

Bits	Bit Name	Access	Reset	Description
23:0	OFFSET[23:0]	R/W	0x800000	**Offset Calibration Bits:** The 24-bit word is signed number in offset binary format. See Calibration section for more information.

GAIN Register

The device has four GAIN registers, each channel has a dedicated GAIN register (see Table 9). This register is 16 bits wide for SIG8892 and 24 bits wide for SIG8893. GAIN register read is allowed anytime, but writing to GAIN register is only allowed while the device is in idle or sleep mode.

Table 14. GAIN Register (Address = 3'b111)

BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT18	BIT 17	BIT 16
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT10	BIT 9	BIT 8
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
GAIN[23]	GAIN[22]	GAIN[21]	GAIN[20]	GAIN[19]	GAIN[18]	GAIN[17]	GAIN[16]
GAIN[15]	GAIN[14]	GAIN[13]	GAIN[12]	GAIN[11]	GAIN[10]	GAIN[9]	GAIN[8]
GAIN[7]	GAIN[6]	GAIN[5]	GAIN[4]	GAIN[3]	GAIN[2]	GAIN[1]	GAIN[0]

Power-On/Reset Value = 0x5555(SIG8892)/0x555555(SIG8893)

Bits	Bit Name	Access	Reset	Description
23:0	GAIN[23:0]	R/W	0x555555	**Gain Calibration Bits:** The 24-bit word is unsigned positive number in binary format. See Calibration section for more information.

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REVISION HISTORY

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please contact to make sure you have the latest revision.

DATE	REVISION	CHANGE
May 20, 2022		Initial release.

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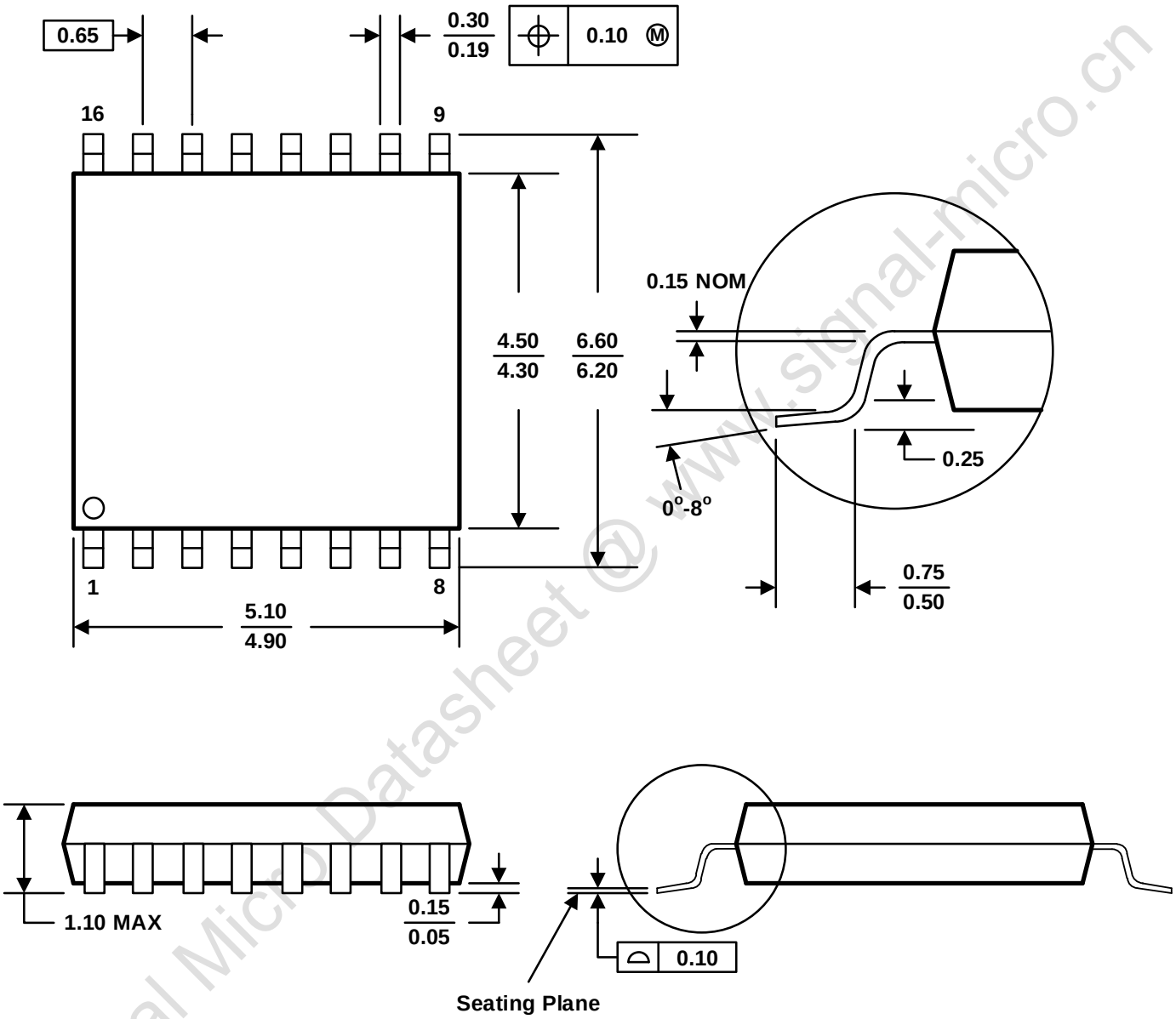
PACKAGE OUTLINE DIMENSIONS



A. Compliant to JEDEC STARDARDS MO-153-AD.
B. All linear dimensions are in millimeters.
C. This drawing is subject to change without notice.

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